

Compal confidential

JBK00 LA-4092P Schematics Document

Mobile AMD S1G2 CPU with ATI
RX781 & SB700 core logic with M82-S

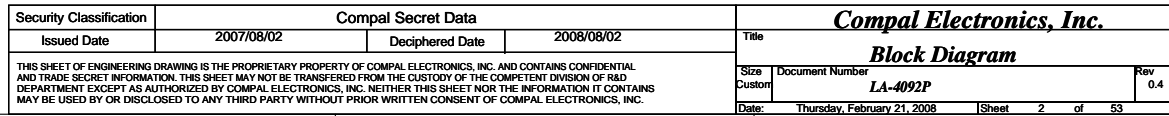
2008-02-20

REV:0.4

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	產出人員
	產出日期
	解密日期

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Consumer AMD UMA/DISCRETE 17"



Voltage Rails

power plane				
State	+B +3VL +5VL	+5VALW +3VALW +1.2VALW +3V_LAN	+1.8V +0.9V	+5VS +3VS +2.5VS +1.8VS +1.5VS +1.1VS +VGA_CORE +1.2V_HT +CPU_CORE_NB +CPU_CORE_0 +CPU_CORE_1
S0	O	O	O	O
S1	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

O MEANS ON X MEANS OFF

I2C / SMBUS ADDRESSING

DEVICE	HEX	ADDRESS
DDR SO-DIMM 0	A0	1 0 1 0 0 0 0 0
DDR SO-DIMM 1	A4	1 0 1 0 0 1 0 0
CLOCK GENERATOR (EXT.)	D2	1 1 0 1 0 0 1 0
ACCELEROMETER	3A	0 0 1 1 1 0 1 0

EC SM Bus1 address

Device	HEX	Address
Smart Battery	16H	0001 011X b
24C16	A0H	1010 000X b
CPU SIC interface	98H	1001 100X b

EC SM Bus2 address

Device	HEX	Address
ADI1032-2 CPU	9AH	1001 101X b
ADI1032-1 VGA	98H	1001 100X b

Symbol Note :



: means Digital Ground

: means Analog Ground

@ : means just reserve , no build

DEBUG@ : means just reserve for debug.

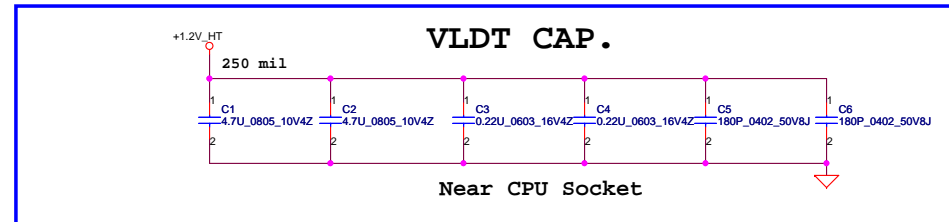
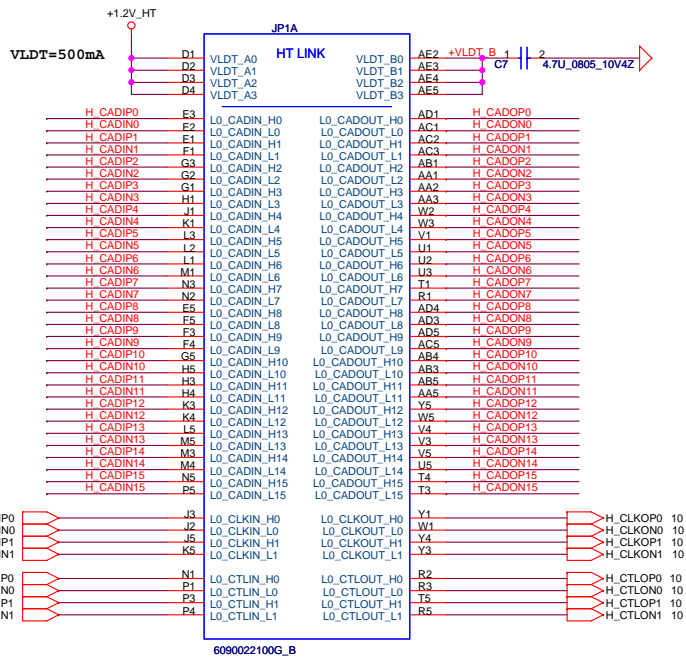


Layout Notes

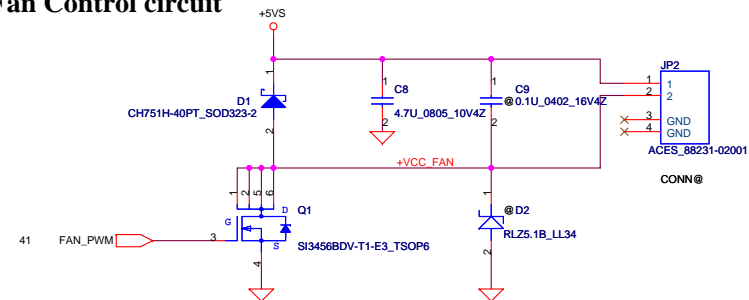
SMBUS Control Table

[illegible]

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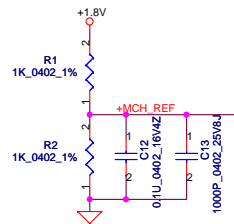


PWM Fan Control circuit

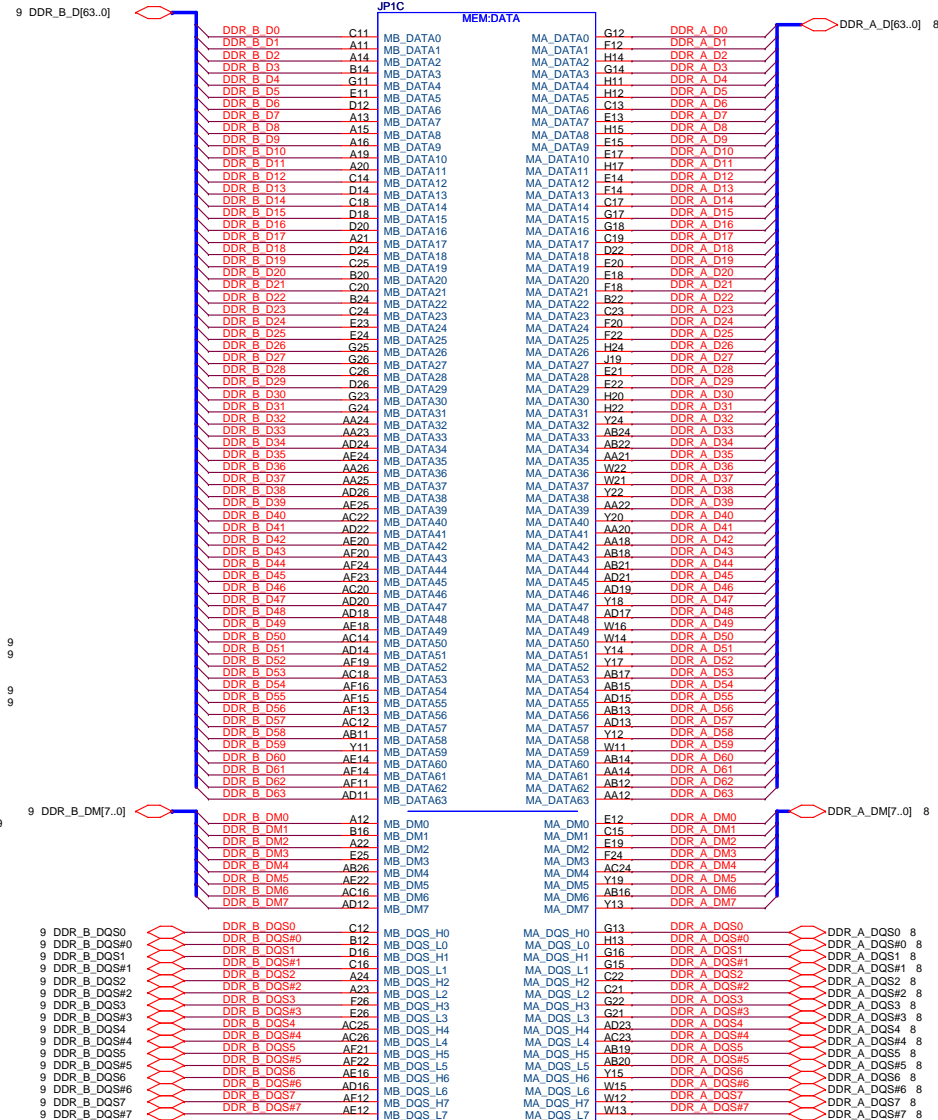
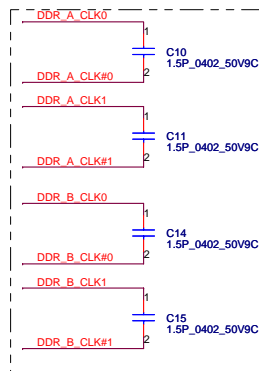


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Processor DDR2 Memory Interface

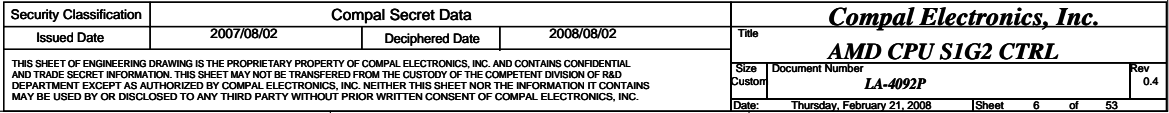


PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH



6090022100G

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VDD(+CPU_CORE) decoupling.

+CPU_CORE_0

C30
330U_X_2VM_R6M

C28
330U_X_2VM_R6M

Near CPU Socket

+CPU_CORE_1

C31
330U_X_2VM_R6M

C29
330U_X_2VM_R6M

Near CPU Socket

+CPU_CORE_0

C32
22U_0805_6.3V6M

C33
22U_0805_6.3V6M

C34
22U_0805_6.3V6M

C35
22U_0805_6.3V6M

Under CPU Socket

+CPU_CORE_1

C36
22U_0805_6.3V6M

C37
22U_0805_6.3V6M

C38
22U_0805_6.3V6M

C39
22U_0805_6.3V6M

Under CPU Socket

+CPU_CORE_0

C40
0.22U_0603_16V4Z

C41
0.01U_0402_25V4Z

C42
180P_0402_50VBJ

Under CPU Socket

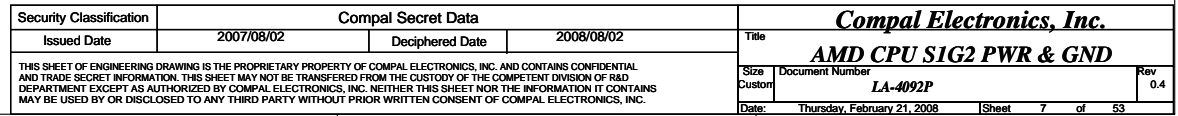
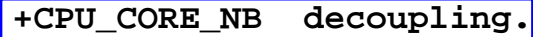
+CPU_CORE_1

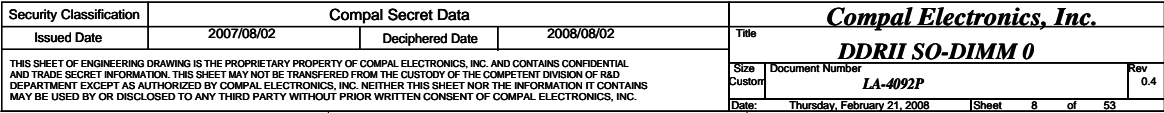
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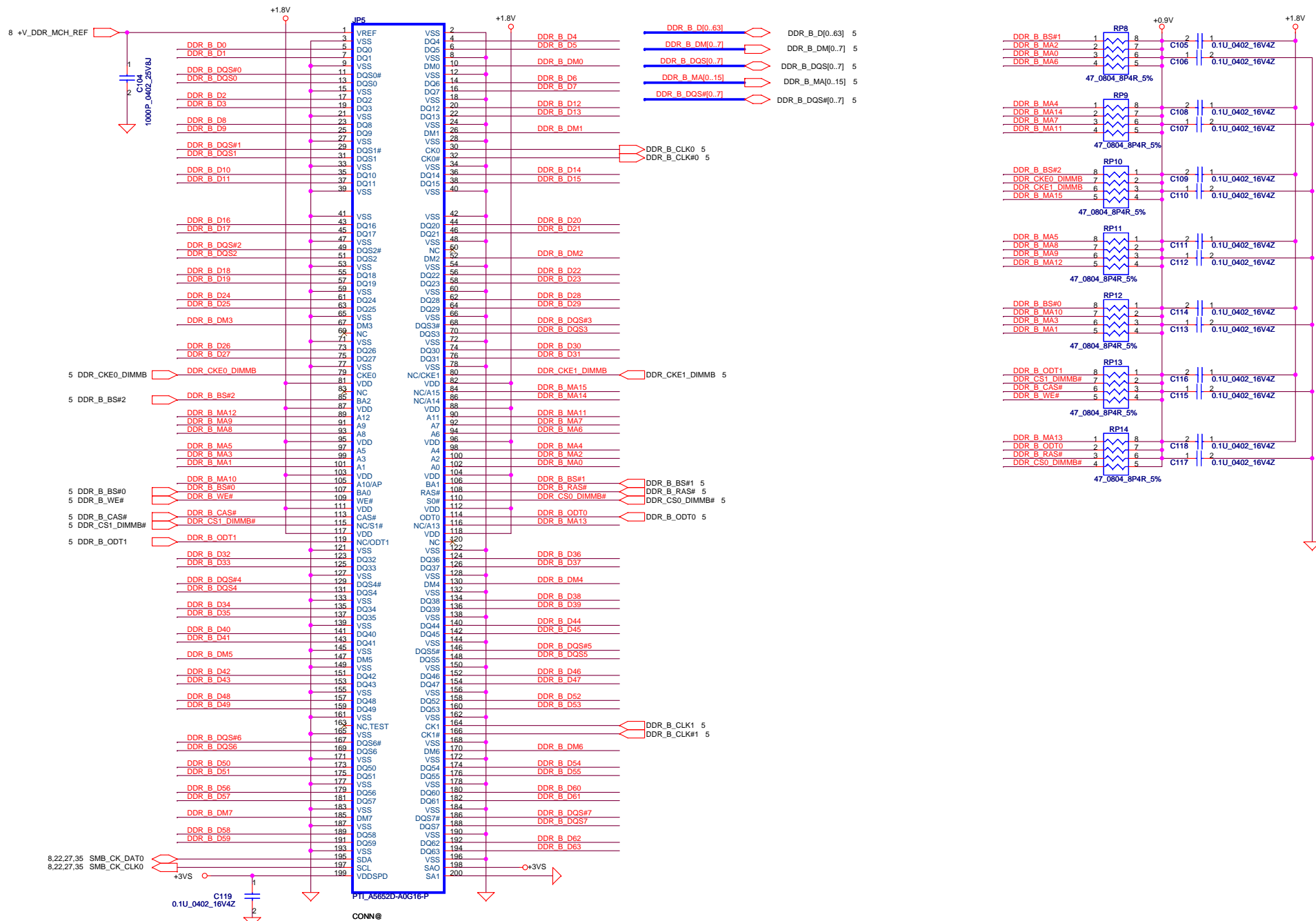
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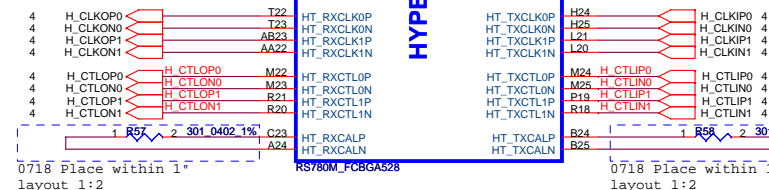
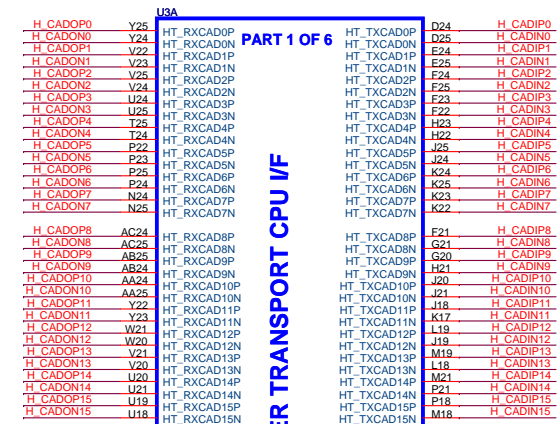
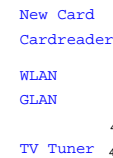
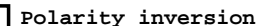
C45
180P_0402_50VBJ

Under CPU Socket

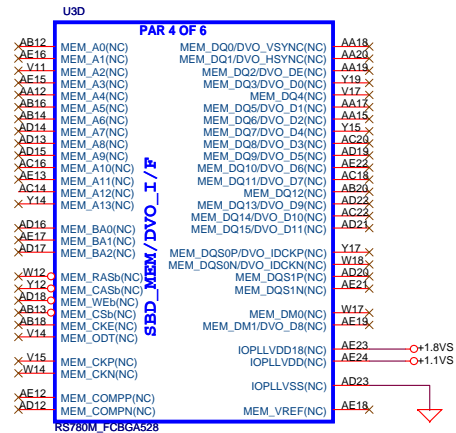


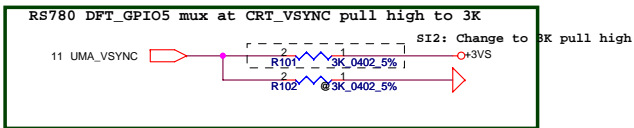






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DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

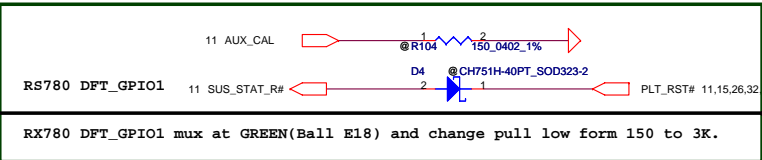
1 : Enable (RX780, RS780)
0 : Disable (RX780, RS780)
PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

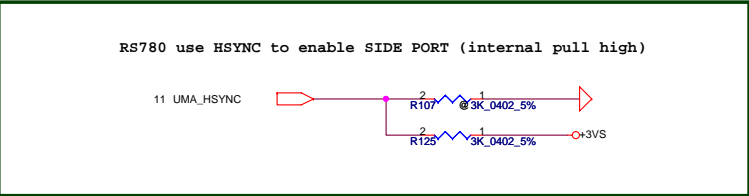
000 : 00001
001 : 00010
010 : 01011
011 : 00100
100 : 01010
101 : 01100
111 : 01011



DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected
RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

RX780: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS780)
0 : Enable (RS780)

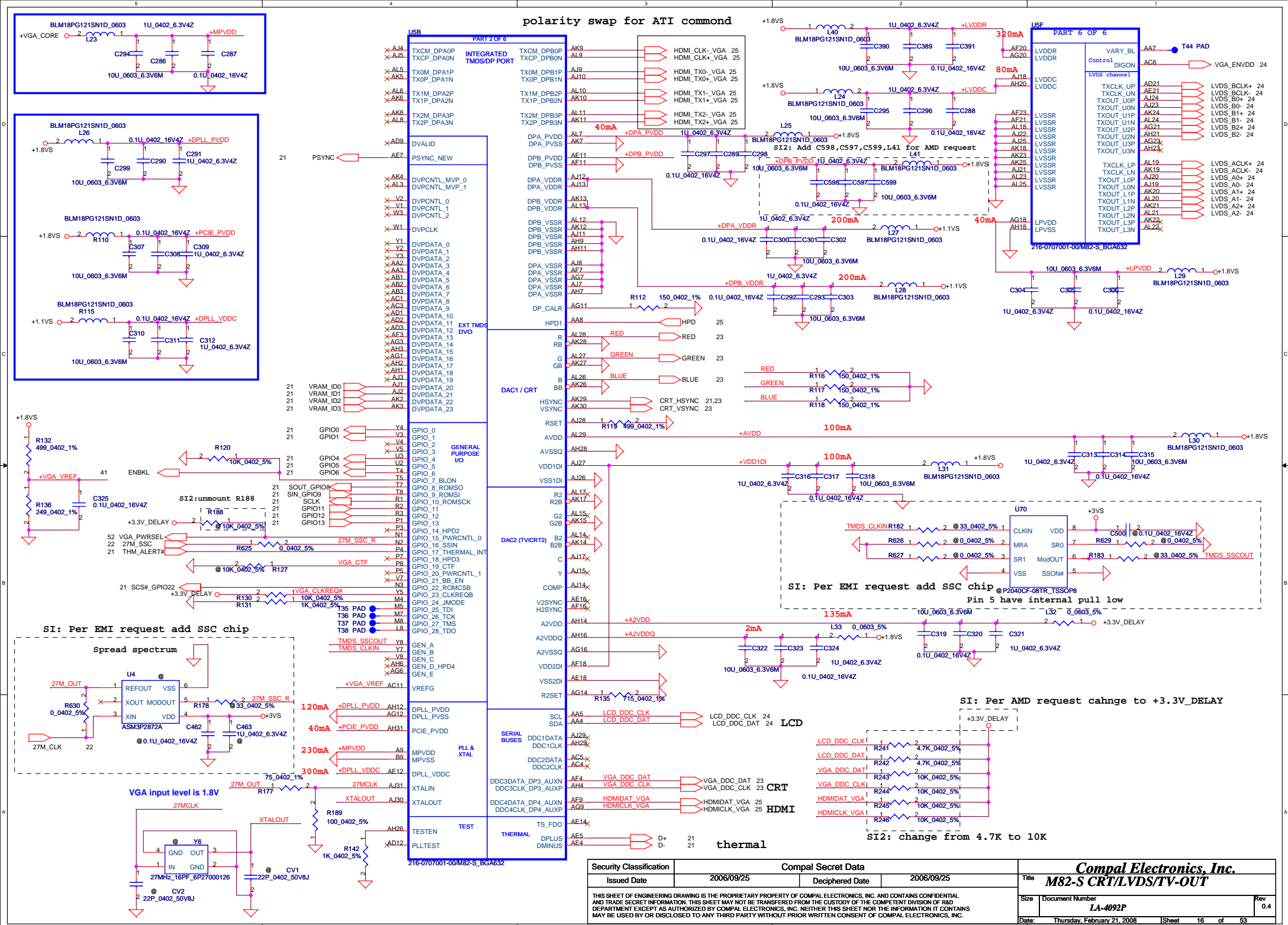
10 PCIE_GTX_C_MRX_P[0..15] < PCIE GTX C MRX P[0..15]
10 PCIE_GTX_C_MRX_N[0..15] < PCIE GTX C MRX N[0..15]
10 PCIE_MTX_C_GRX_P[0..15] < PCIE MTX C GRX P[0..15]
10 PCIE_MTX_C_GRX_N[0..15] < PCIE MTX C GRX N[0..15]

PCIE LANE REVERSAL



PCIE LANE REVERSAL

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Security Classification	Compal Secret Data			Compal Electronics, Inc. Title M82-S CRT/LVDS/TV-OUT		
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20 MDA[63..32] MDA[63..32]
19 MDA[31..0] MDA[31..0]

MEMORY
INTERFACE

USC
Part 3 of 6

write strobe read strobe

MAA[12..0] MA[12..0] 19,20
BA[2..0] BA[2..0] 19,20

DQMA# [3..0] 19

DQMA# [7..4] 20

QSA [3..0] 19

QSA [7..4] 20

QSA# [3..0] 19

QSA# [7..4] 20

ODTA0 19
ODTA1 20

CLKA0 19
CLKA1 20

CLKA0# 19
CLKA1# 20

RASA#0 19
RASA#1 20

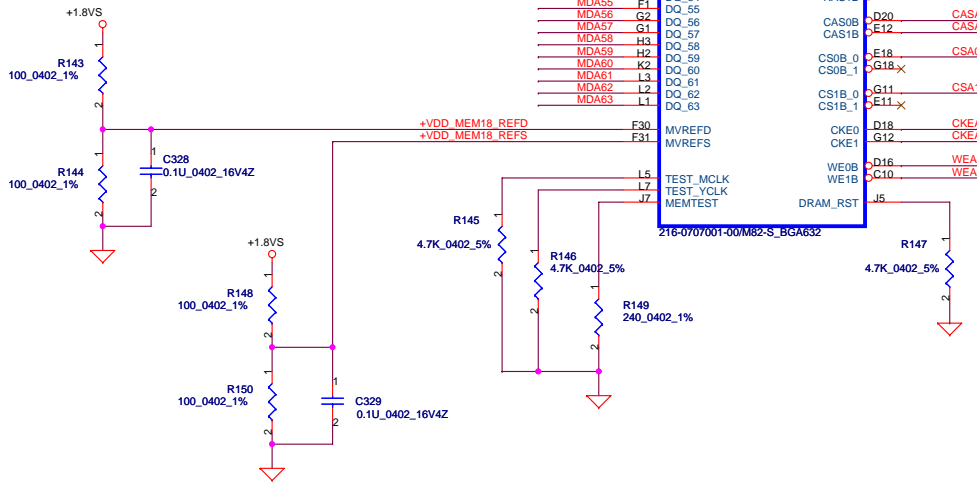
CASA#0 19
CASA#1 20

CSA# 19

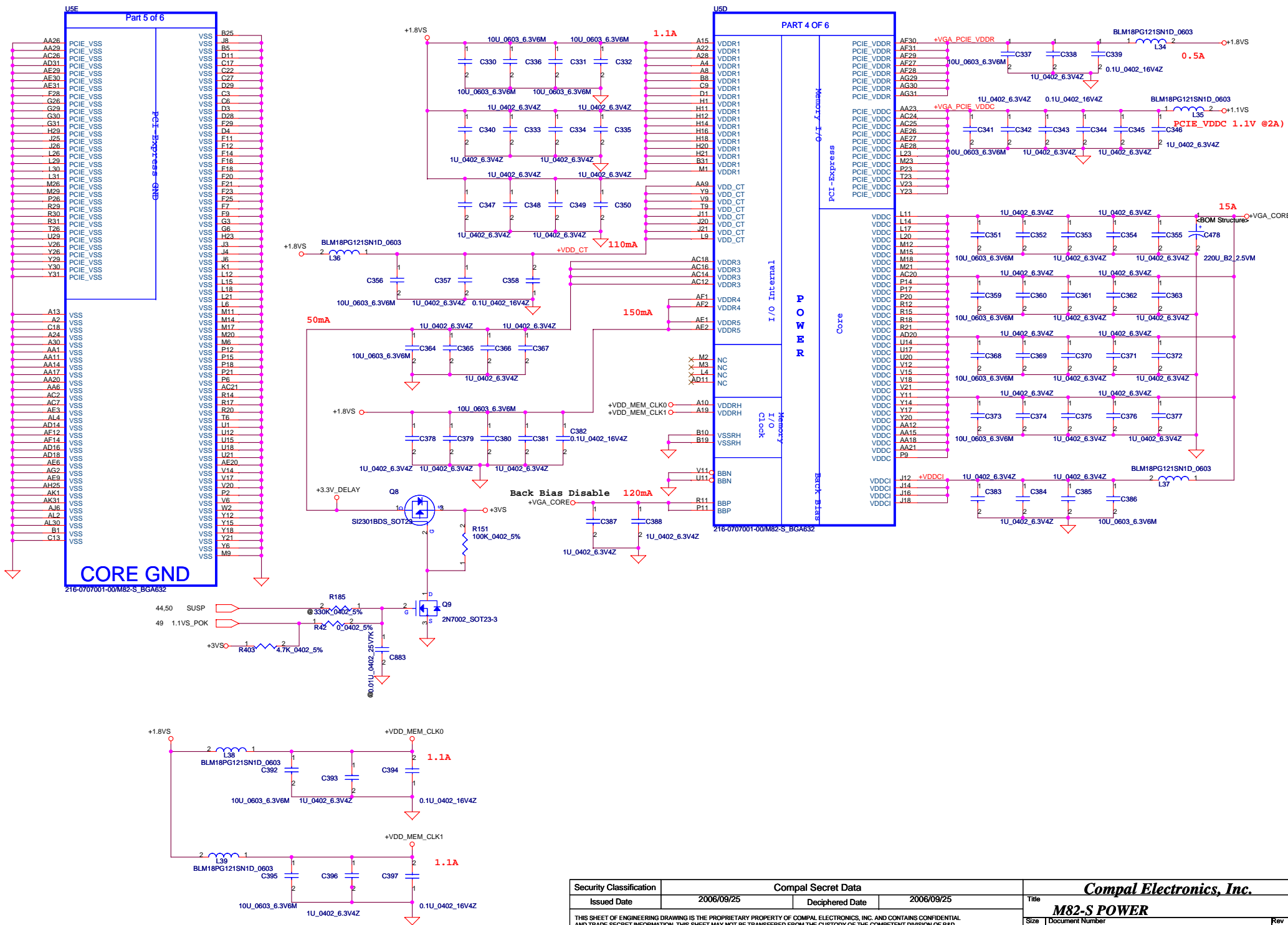
CSA1# 20

CKEA0 19
CKEA1 20

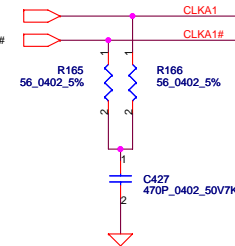
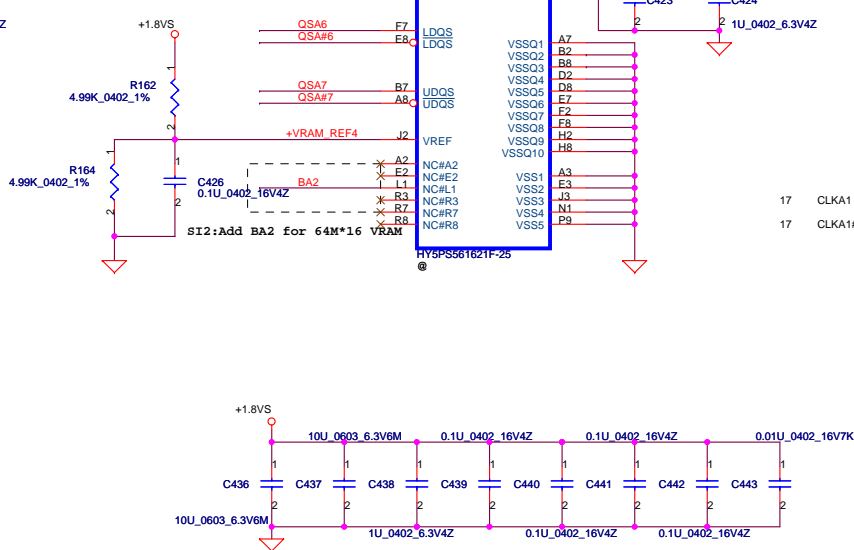
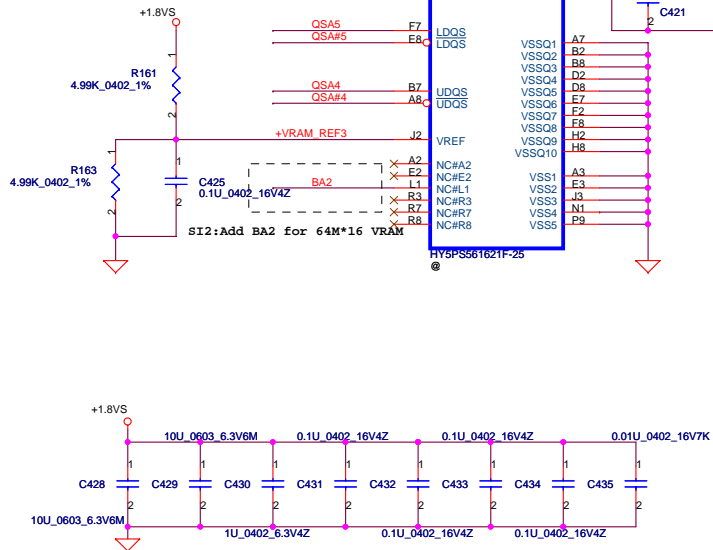
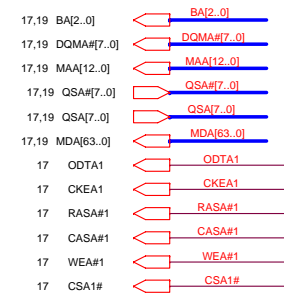
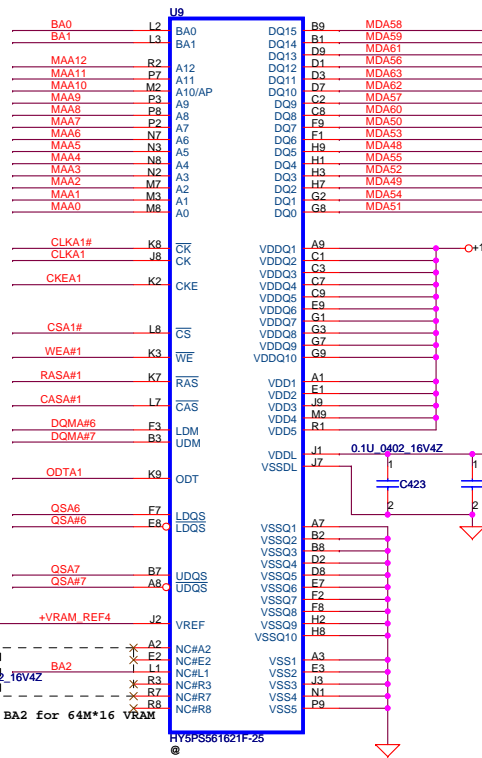
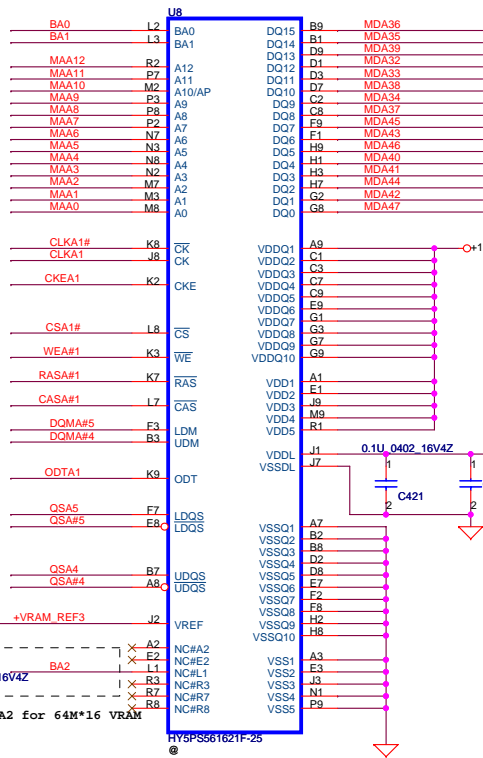
WEA#0 19
WEA#1 20



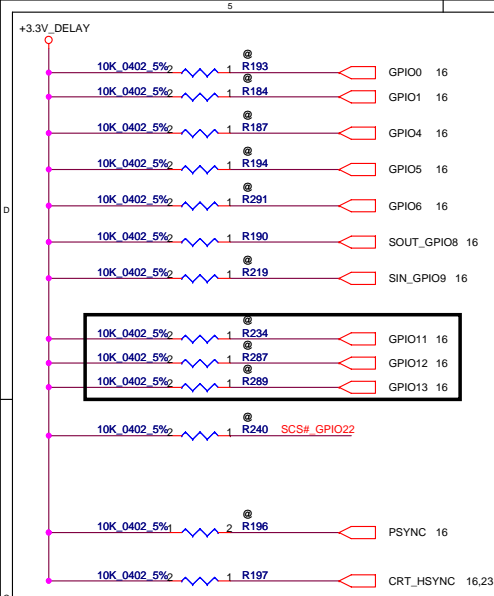
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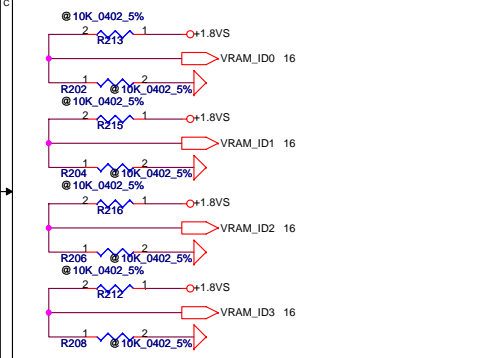
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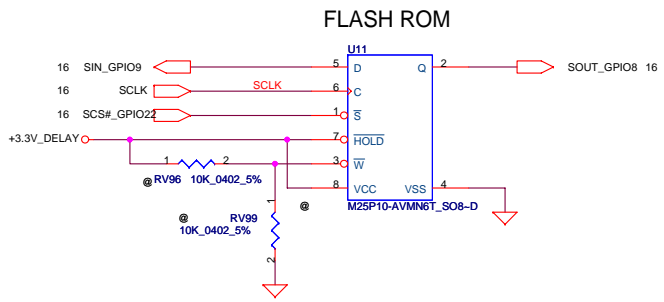
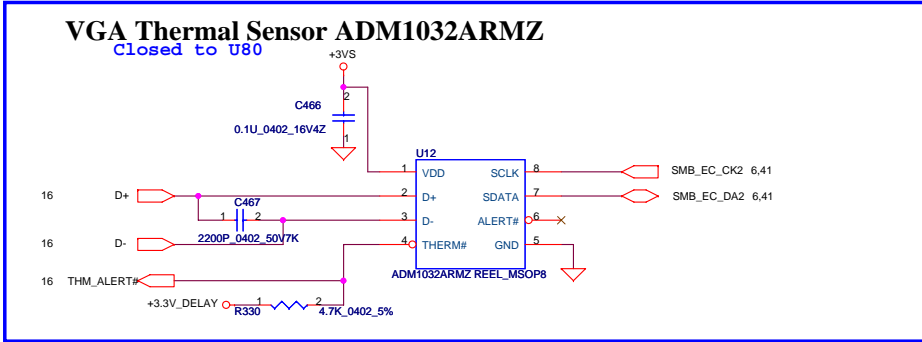


GPIO9 = 0 (BIOS_ROM_EN = 0)		
GPIO[13:11]		MEMORY SIZE
<i>0 0 0</i>		128MB
<i>0 0 1</i>		256MB
<i>0 1 0</i>		64MB
<i>1 0 0</i>		512MB

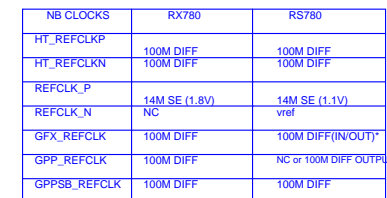
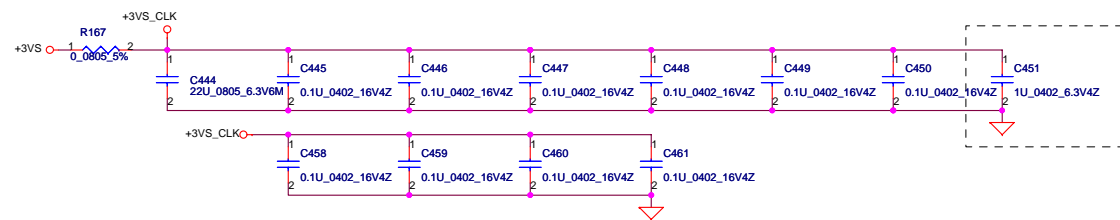


STRAPS	PIN	DESCRIPTION OF RECOMMENDED SETTING	RECOMMENDED M8X
TX_PWRS_ENB	GPIO0	PCIE FULL TX OUTPUT SWING	0
TX_DEEMPH_EN	GPIO1	PCIE TRANSMITTER DE-EMPHASIS ENABLES	0
BIF_DEBUG_ACCESS	GPIO4	DEBUG SIGNALS MUXED OUT	0
BIF_GEN2_EN_A	GPIO5	PCI-E 5.0GT/s or 2.5 GT/s select	0
DEBUG_I2C_ENABLE	GPIO6	Internal use only	0
BIF_AUDIO_EN	GPIO8	ENABLE HD AUDIO(M8X)	1
ROMIDCFG[3:0]	GPIO [9,13,12,11]	SERIAL ROM TYPE OR MEMORY APERTURE SIZE SELECT	0 1 0 1
BIOS_ROM_EN	GPIO_22_ROMCSB	DISABLE EXTERNAL BIOS ROM	0
BIF_VGA_DIS	PSYNC	VGA ENABLED==0 is enable	0
BIF_HDMI_EN	HSYNC	HDMI ENABLE	1
VRAM_ID[3:0]	DVDPDATA (23,22,21,20)		VRAM_ID 3,2,1,0
		Samsung 64Mx16 1.8V	0 0 0 0
		Samsung 32Mx16 1.8V	0 0 0 1
		Hynix 64Mx16 1.8V	0 0 1 0
		Hynix 32Mx16 1.8V	0 0 1 1
		Qimonda 32Mx16 1.8V	0 1 0 0
		Qimonda 64Mx16 1.8V	0 1 0 1

ATI RESERVED CONFIGURATION STRAPS			
ALLOW FOR PULLUP PADS FOR THESE STRAPS AND IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESE			
GPIO2	GPIO3	GPIO5	GPIO6
DVALID	H2SYNC	V2SYNC	
PULLUP PADS ARE NOT REQUIRED FOR THESE STRAPS BUT IF THESE GPIOS ARE USED, THEY MUST NOT CONFLICT DURING RESET			
GENERICC	GPIO21_BB_EN	GPIO_28_TDO	



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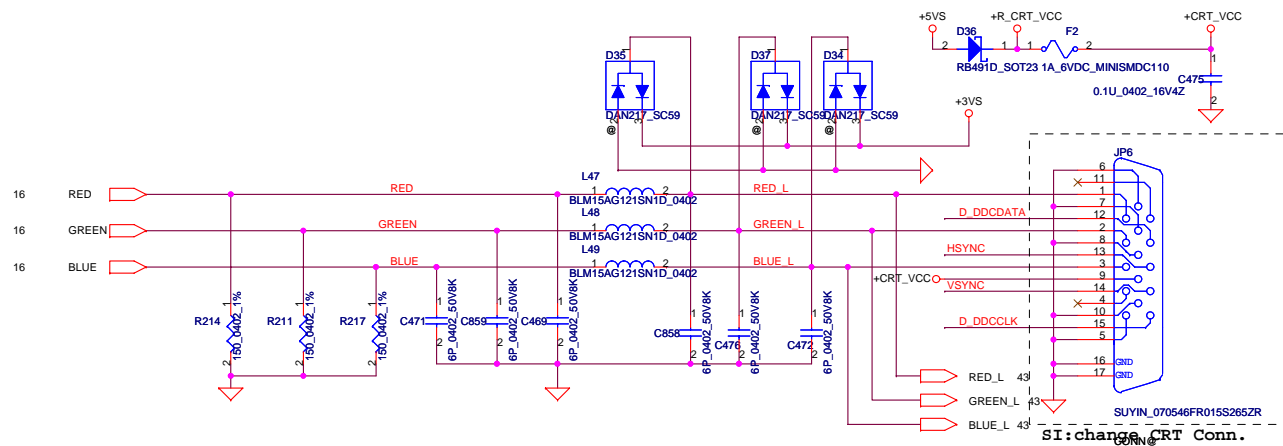


NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0*	configure as differential 100MHz output

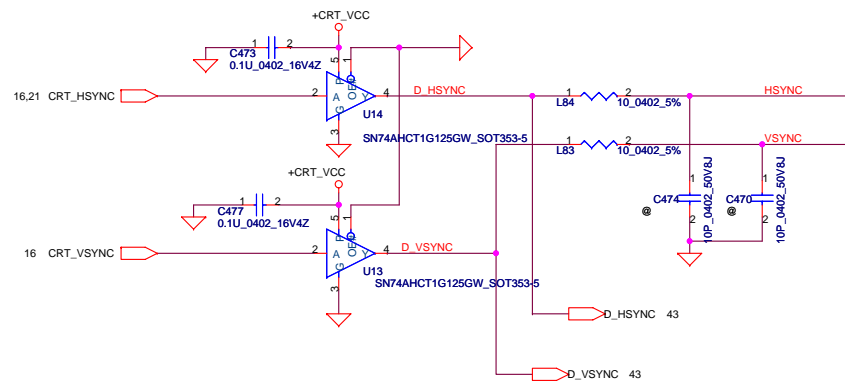
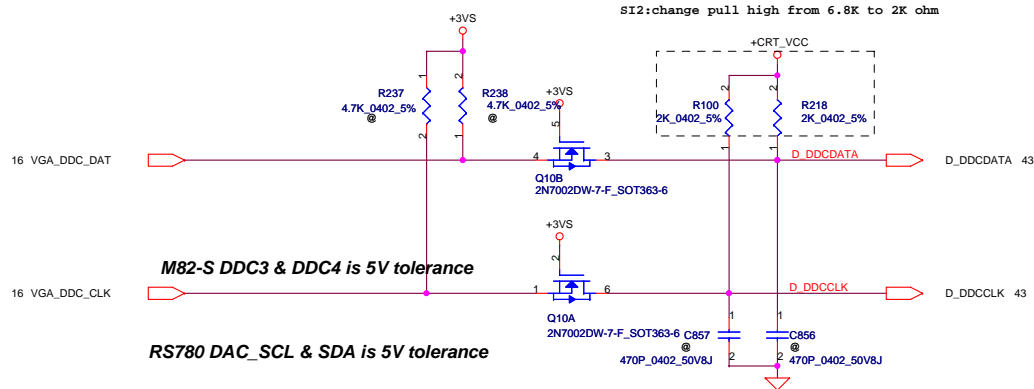
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<p align="center"><i>Compal Electronics, Inc.</i></p>		
<p align="center"><i>Clock generator</i></p>		
Title		
Size	Document Number	Rev
Custom	<i>LA-4092P</i>	<i>0.4</i>
Date:	Thursday, February 21, 2008	Sheet 22 of 53

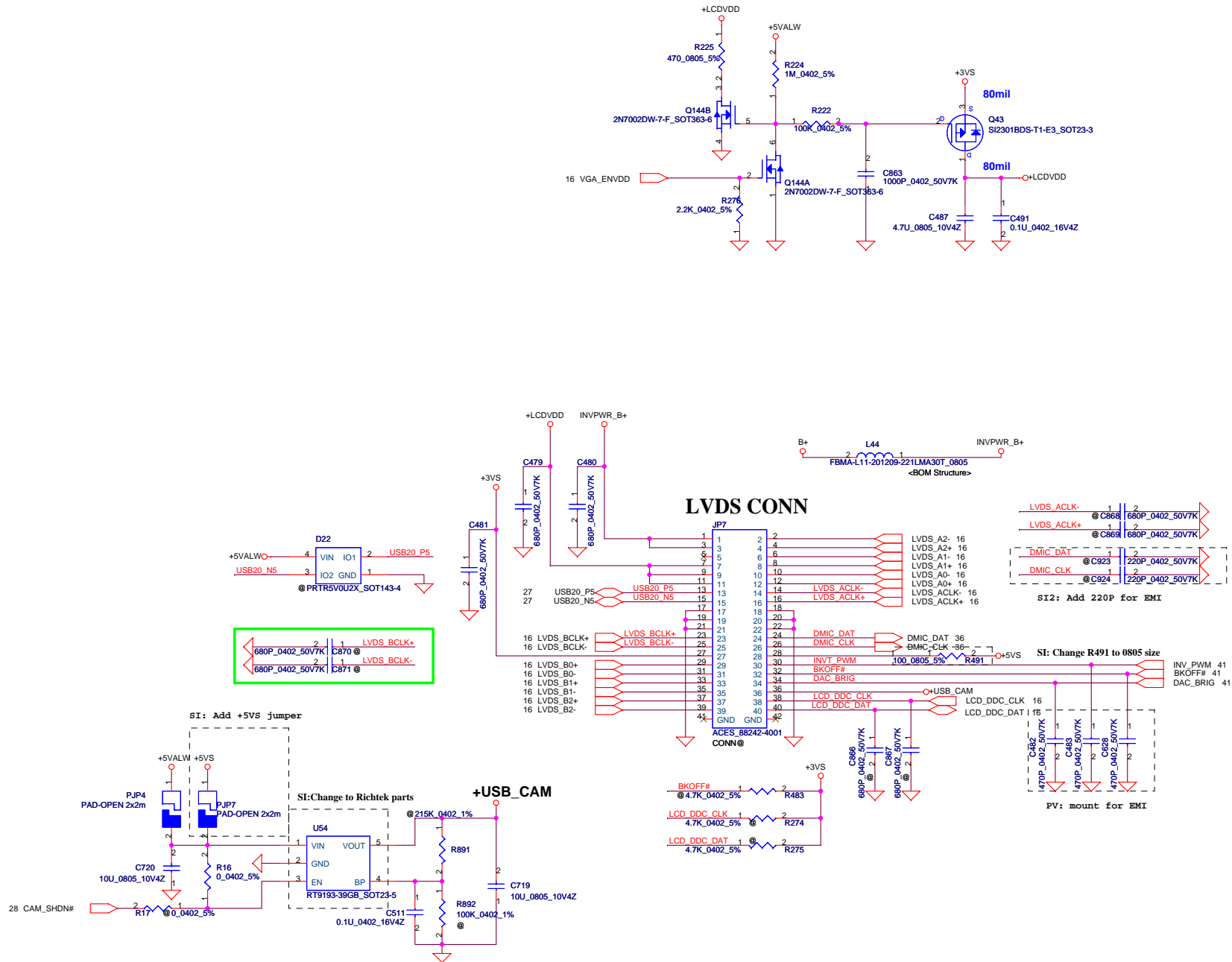
CRT CONNECTOR



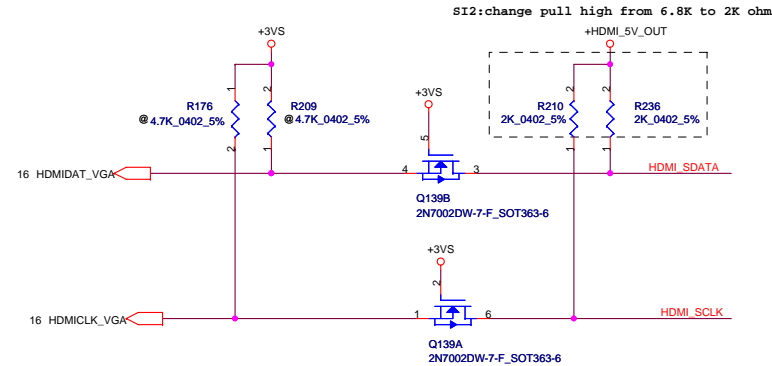
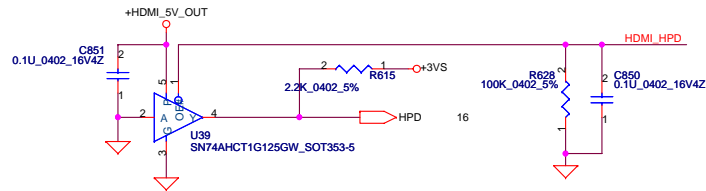
SI2:change pull high from 6.8K to 2K ohm



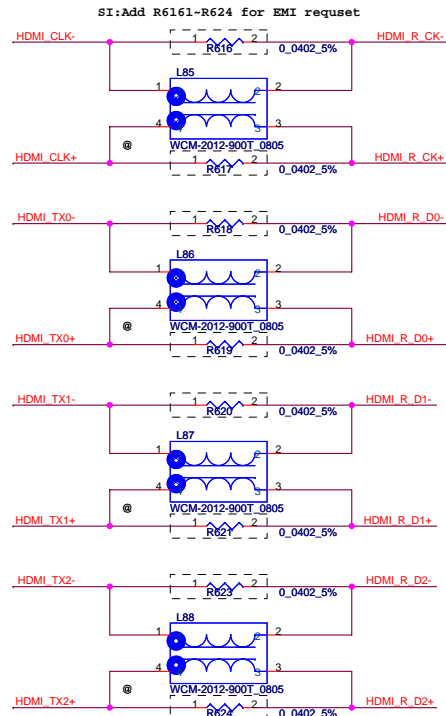
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	CRT Connector	
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				Custom	LA-4092P
Date: Thursday, February 21, 2008				Sheet	23 of 53



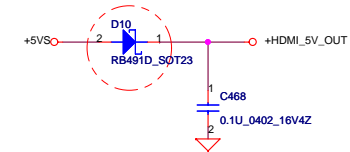
Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
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				Custom	LA-4092P
				Date:	Thursday, February 21, 2008
				Sheet	24 of 53
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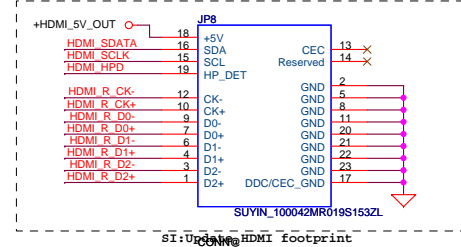
C:Chg. PN to SB770020010.



MP: Update D10 to meet HDMI.

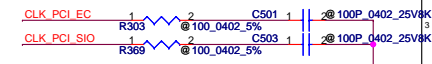
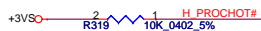


HDMI Connector



SI: Update HDMI footprint

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				Rev	0.4
				Date:	Thursday, February 21, 2008
				Sheet	25 of 53

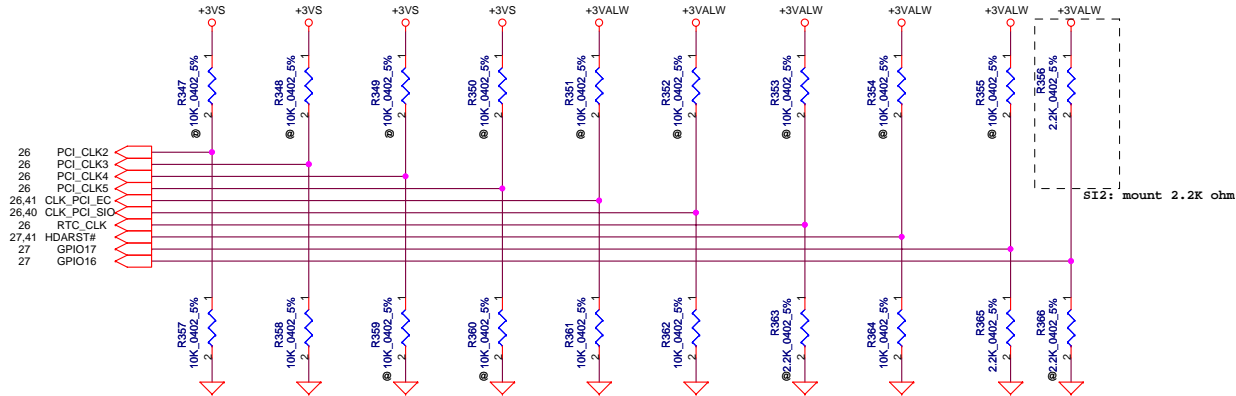


Security Classification	Compal Secret Data			Compal Electronics, Inc. SB700-PCIE/PCI/ACPI/LPC/RTC		
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title		
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				Date:	Thursday, February 21, 2008	Sheet 26 of 53

REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

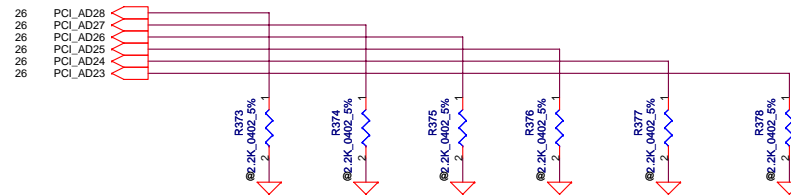
	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		



DEBUG STRAPS

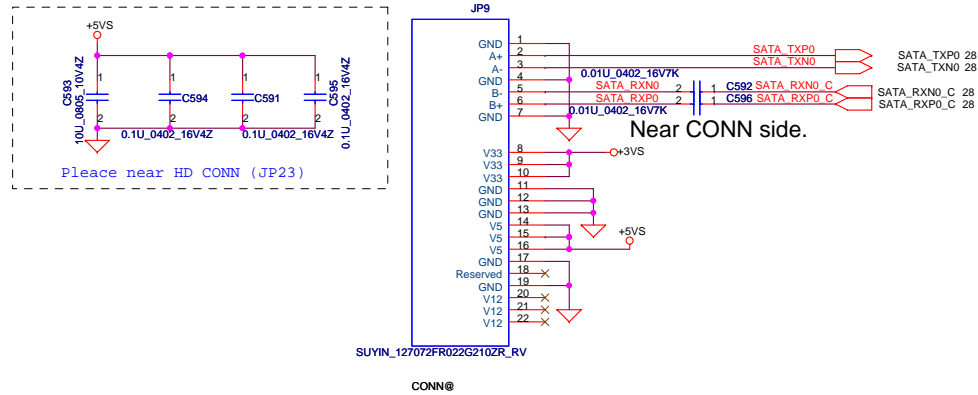
SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

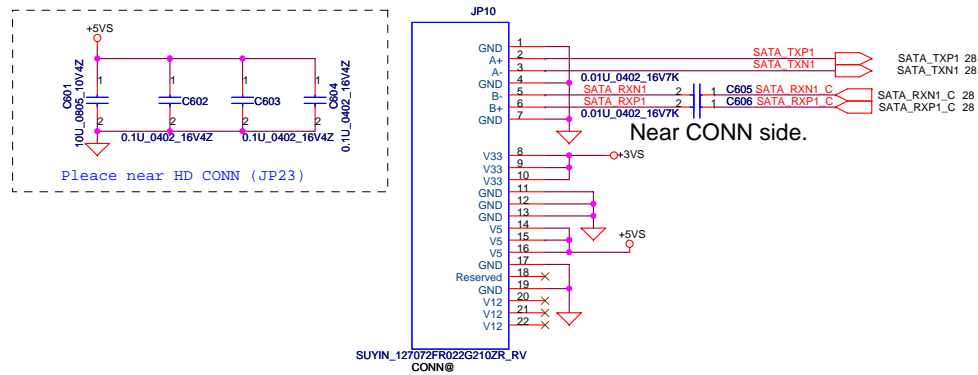


Security Classification		Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	SB700 STRAPS	
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				Rev	0.4

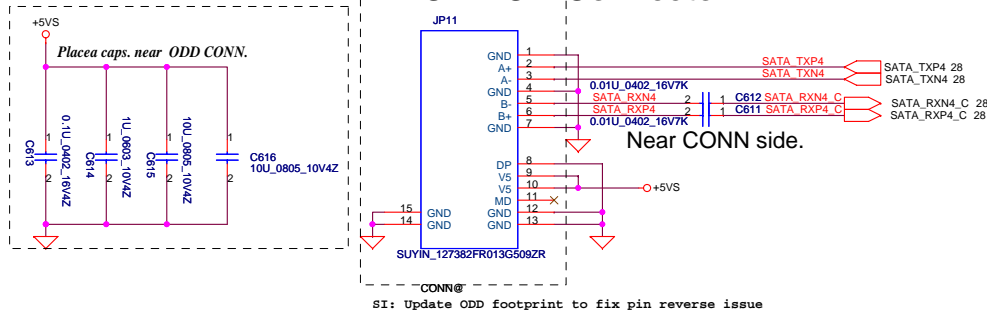
HDD Connector



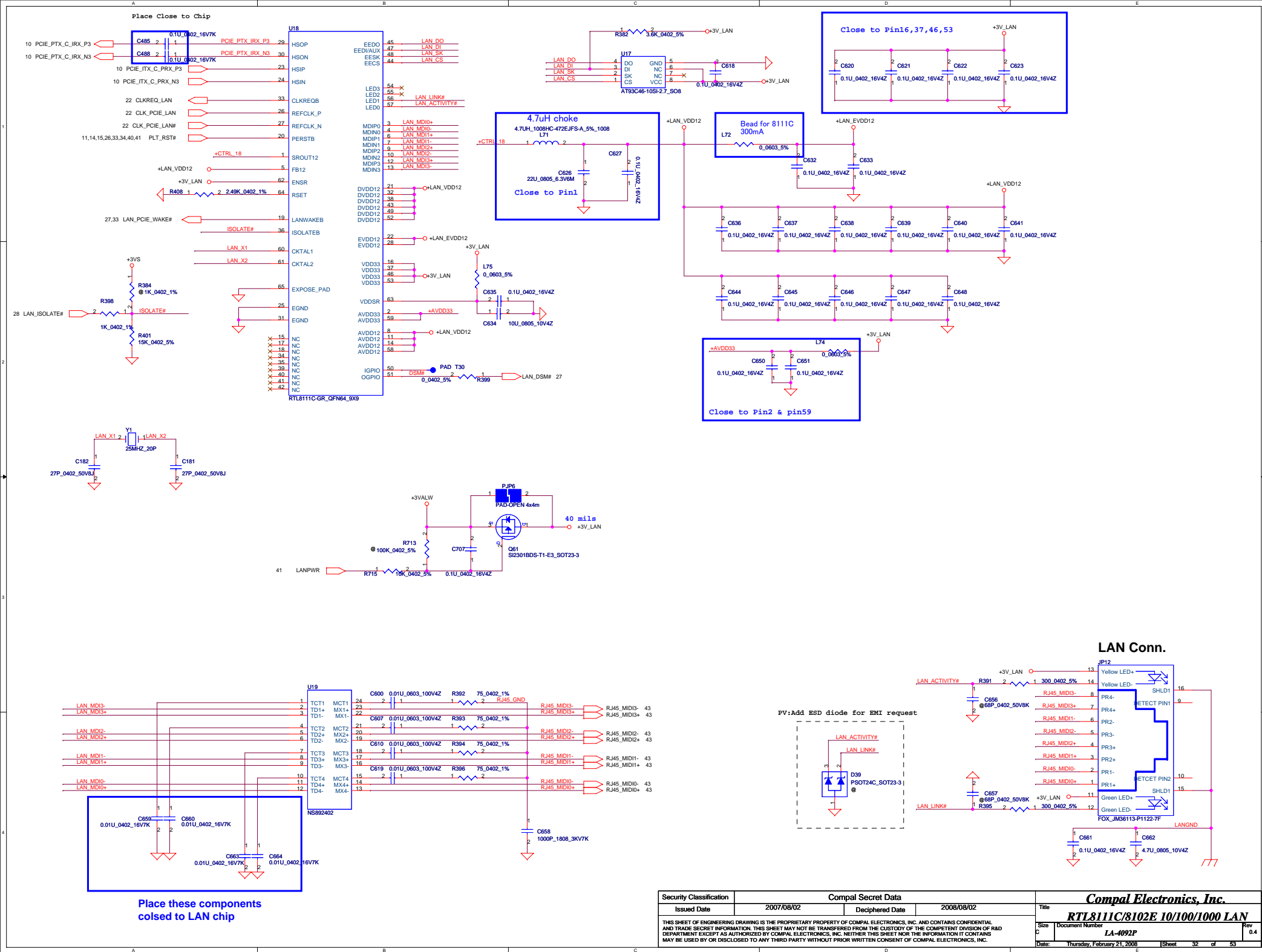
2nd HDD Connector-option



CD-ROM Connector



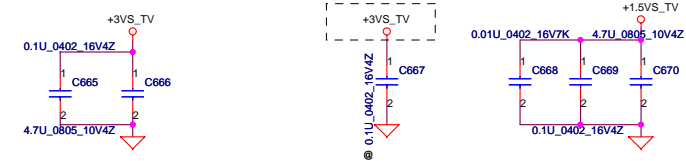
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	Compal Electronics, Inc.	
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				Custom	0.4
				Document Number	LA-4092P
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				Sheet	31 of 53



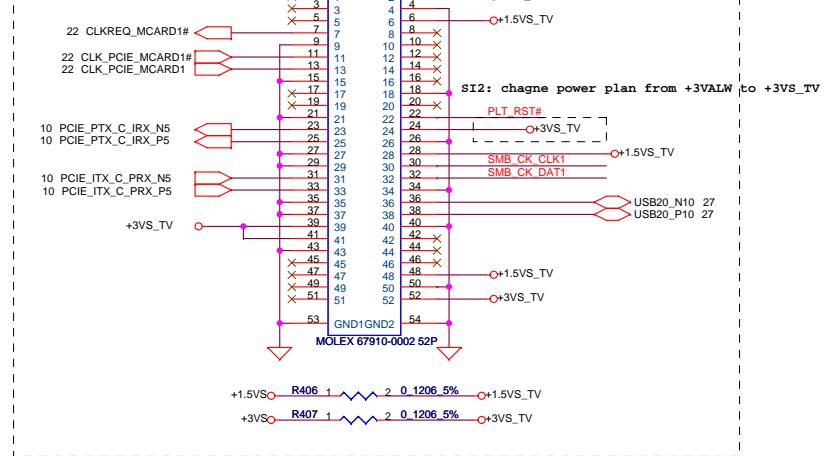
Security Classification	Compal Secret Data			Compal Electronics, Inc. RTL8111C/8102E 10/100/1000 LAN		
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Title		
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Mini Card---TV tuner

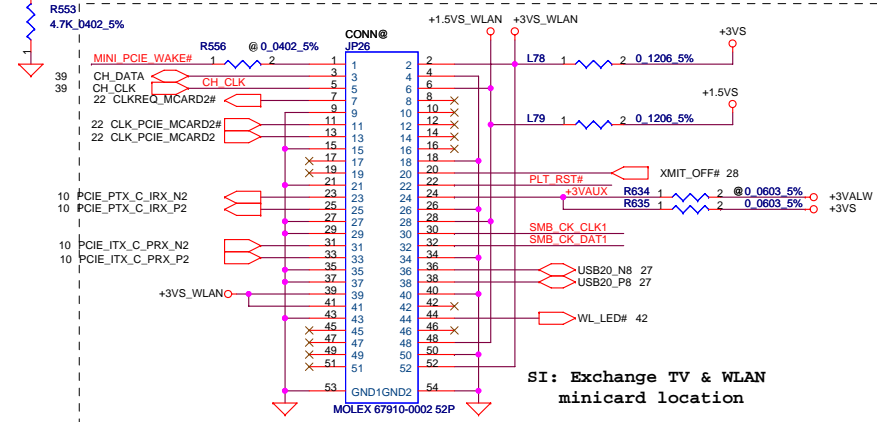
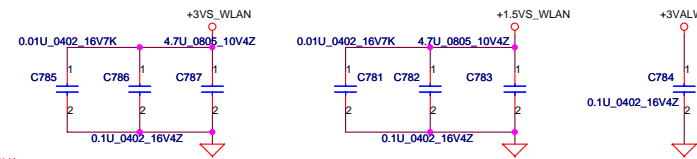
SI2: chagne power plan from +3VALW to +3VS_TV



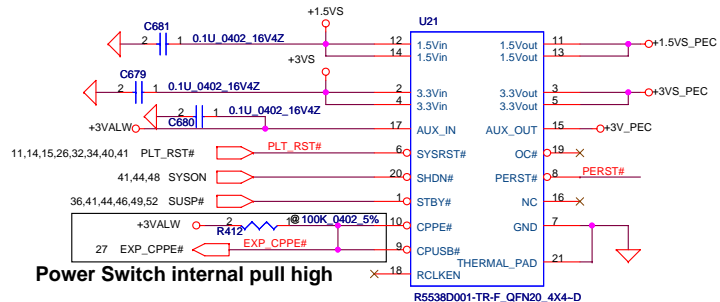
SI: Exchange TV & WLAN minicard location



Mini-Express Card---WLAN



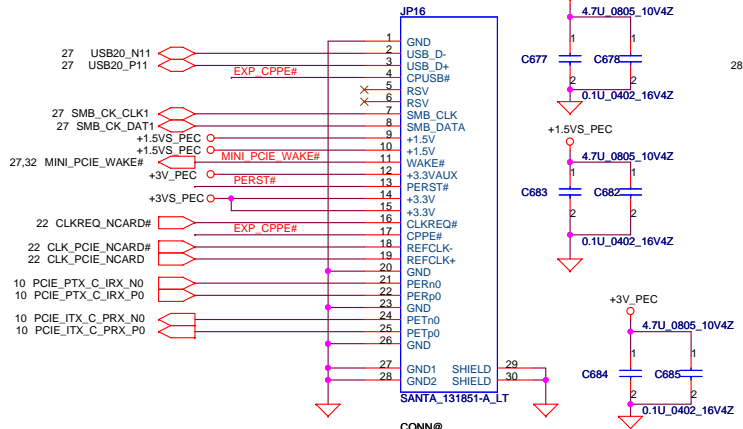
New Card



Power Switch internal pull high

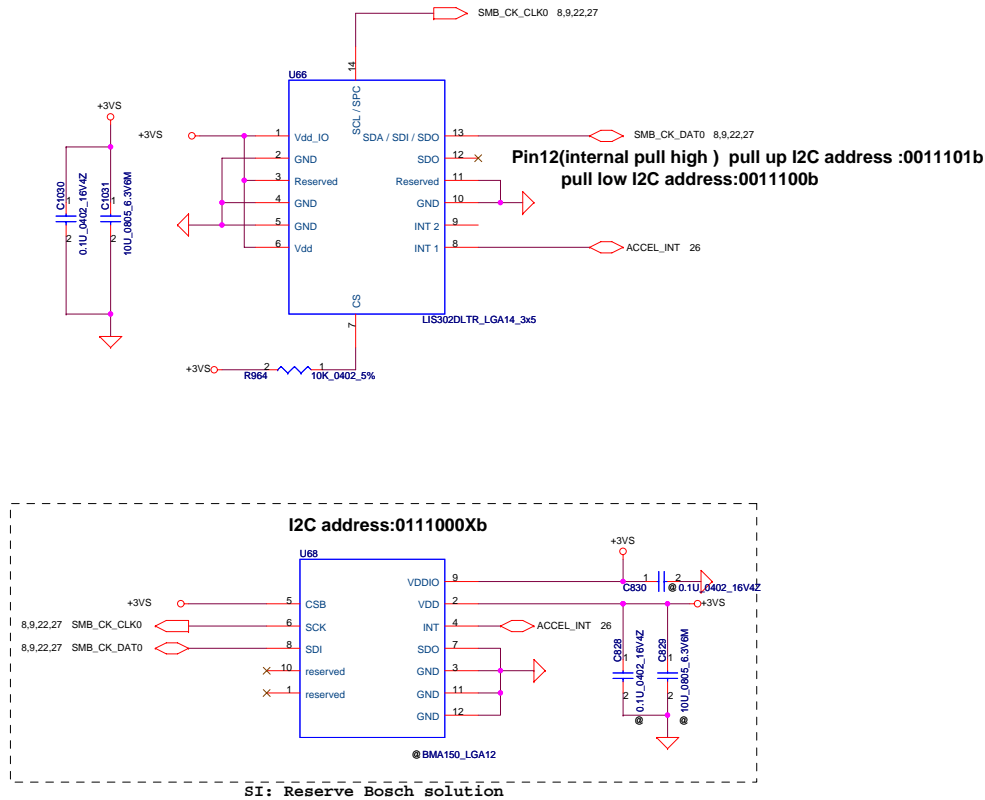
USE TI TPS2231MRGPR

Near to Express Card slot.



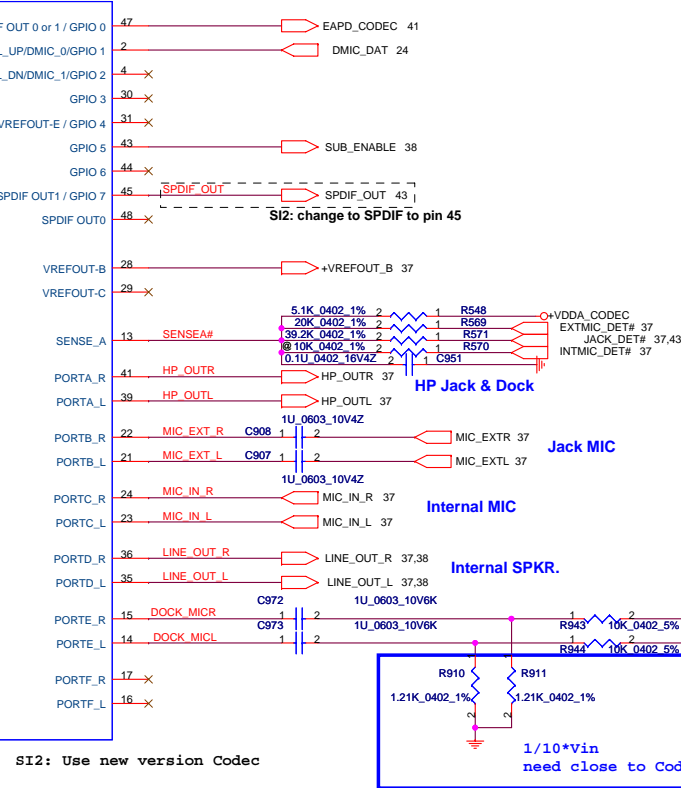
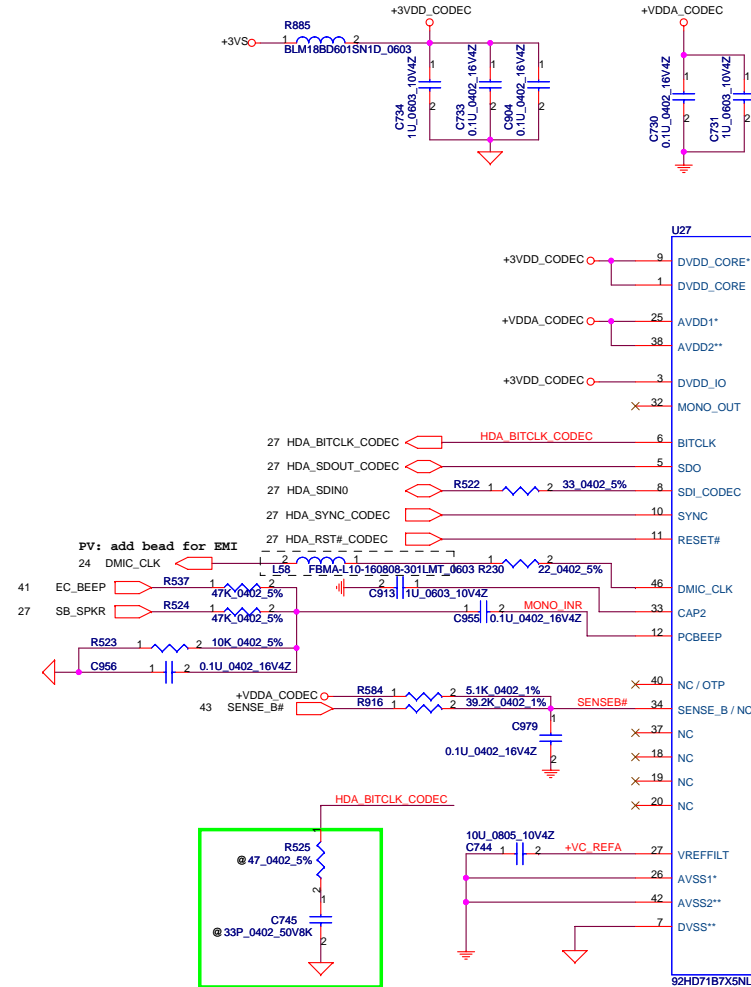
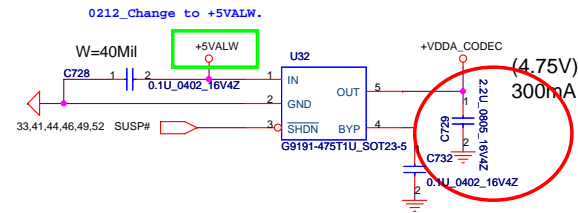
Security Classification	Compal Secret Data		Title	
Issued Date	2007/08/02	Deciphered Date	2008/08/02	Mini-Card/Mini-PCI/Express Card
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ACCELEROMETER

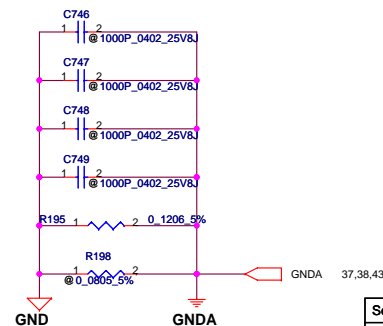


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Issued Date	2006/08/04	Deciphered Date	2006/10/06	Title
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CODEC POWER

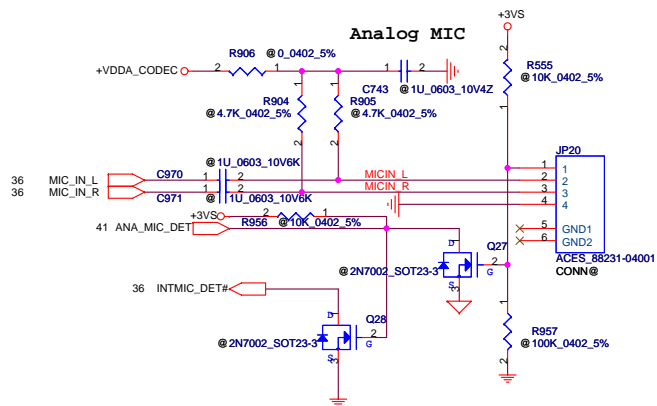
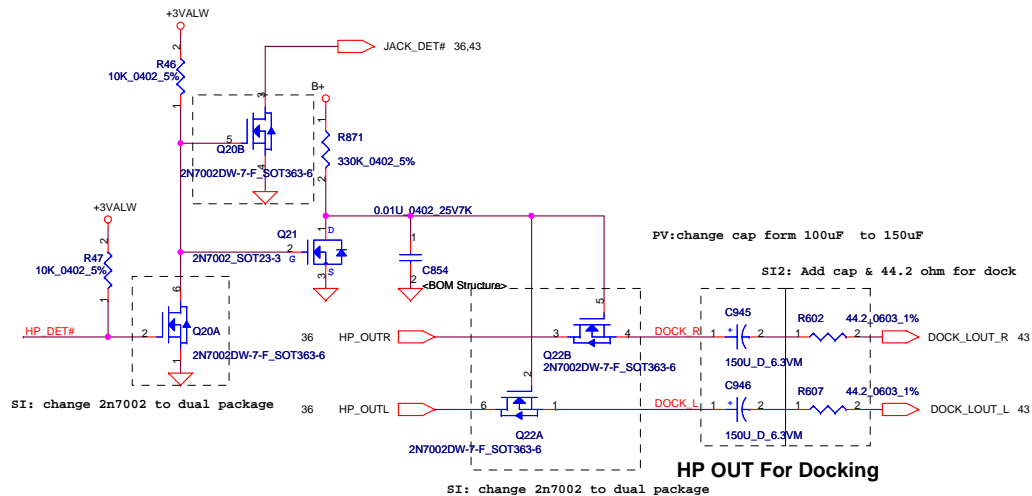
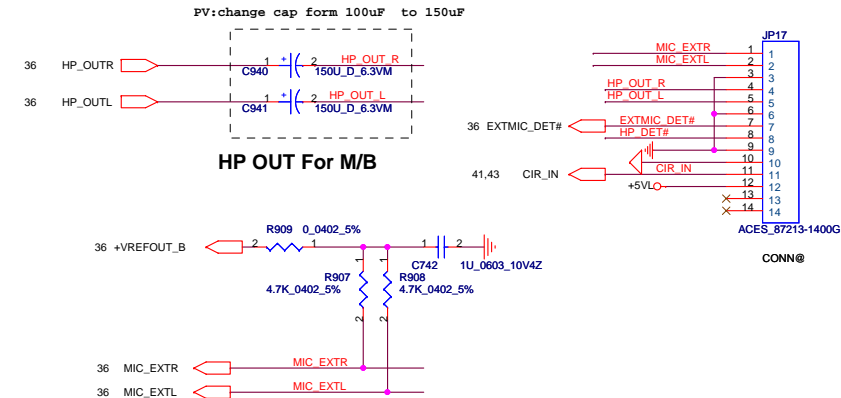
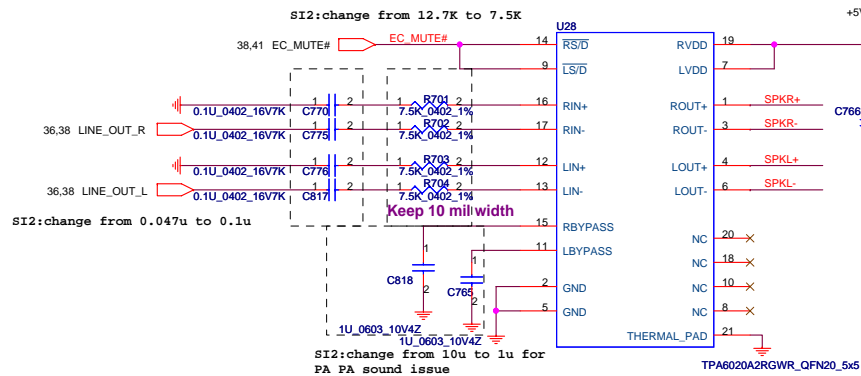


SENSE A		SENSE B	
Port	Resistor	Port	Resistor
A	39.2K	E	39.2K
B	20K	F	20K
C	10K	G	10K
D	5.11K	H	5.11K

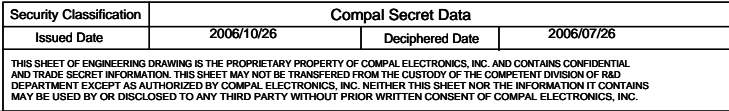


HP_DET#	MIC_DET	LINEOUT	PORT-A <Earphone OUT>	MIC	EQ
0 (LOW)	0 (LOW)	OFF	ON	ON	Disable
0 (LOW)	NC	OFF	ON	OFF	Disable
NC	0 (LOW)	ON	OFF	ON	Enable
NC	NC	ON	OFF	OFF	Enable

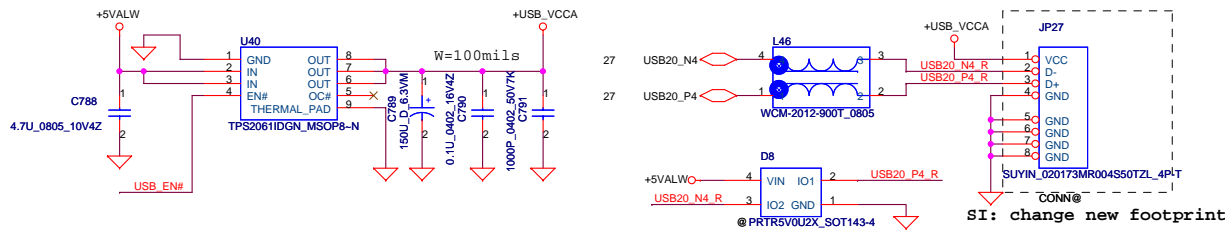
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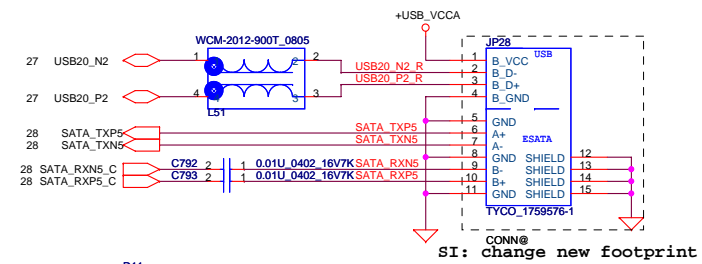
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Deciphered Date				2008/08/02				AMP & Audio Jack			
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				Custom				0.4			
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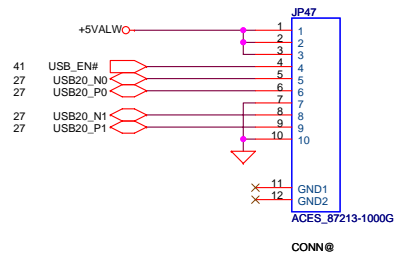
Left side USB CONNECTOR 0



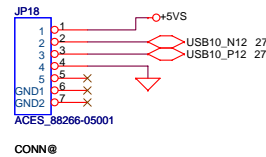
Left side ESATA/USB combination Connector



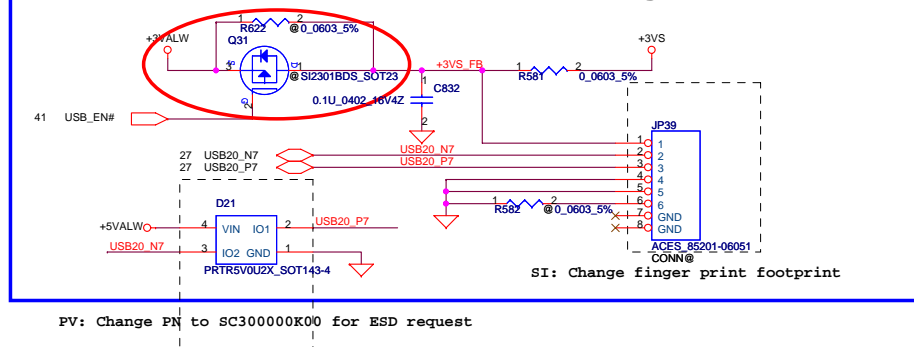
USB Board Conn



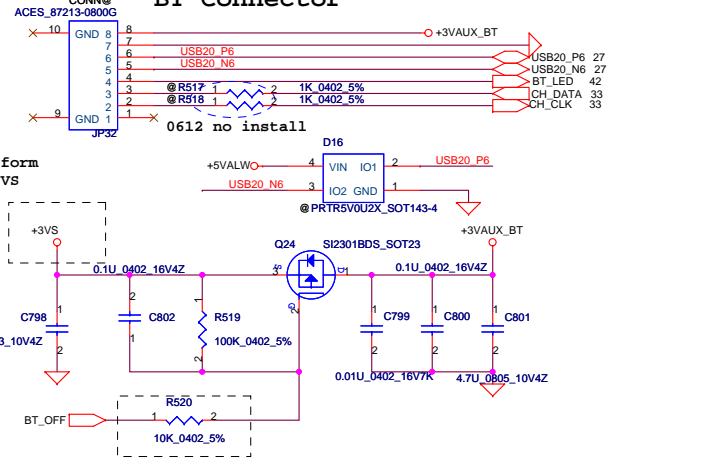
Touch screen



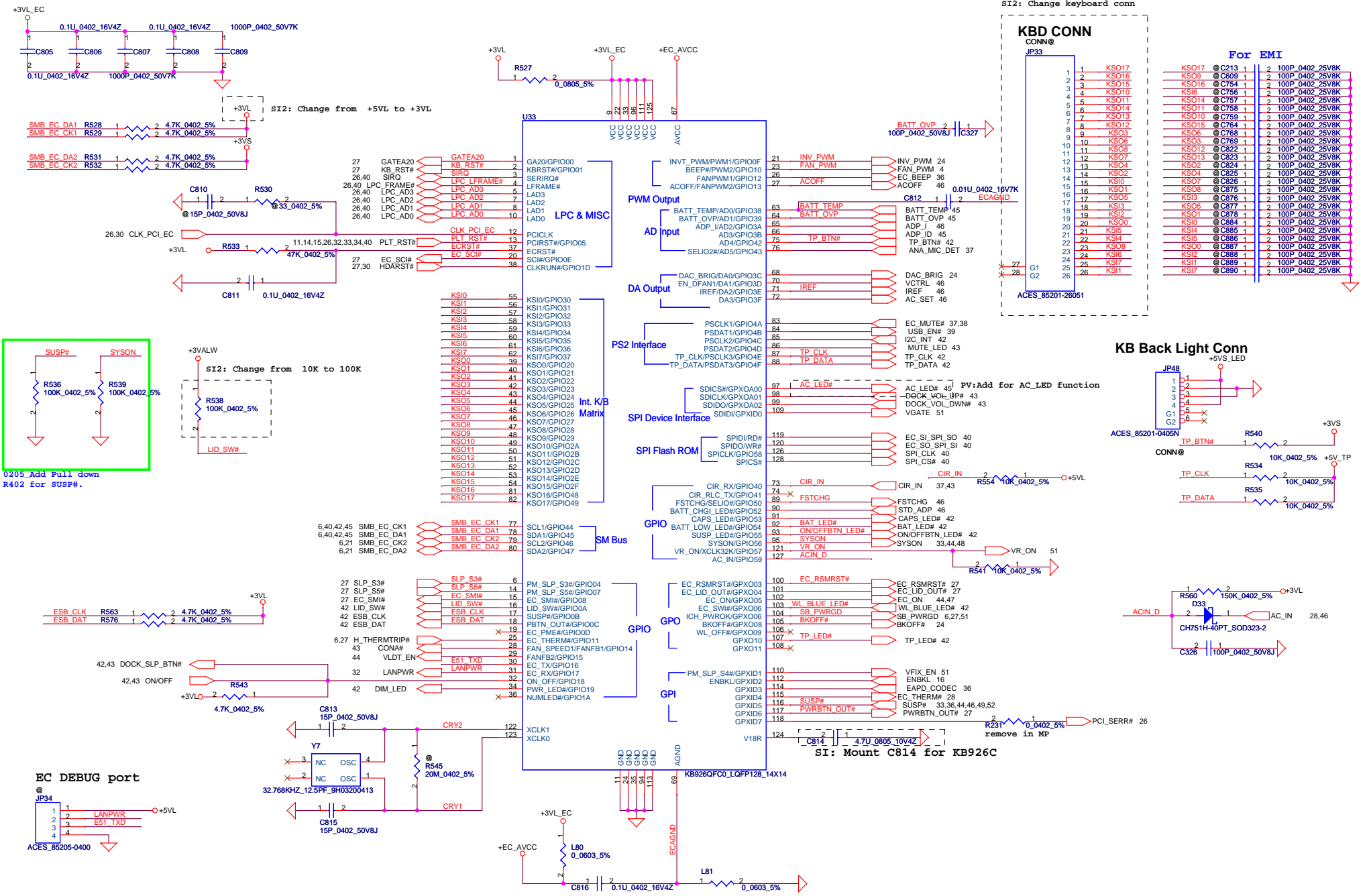
Finger printer



BT Connector



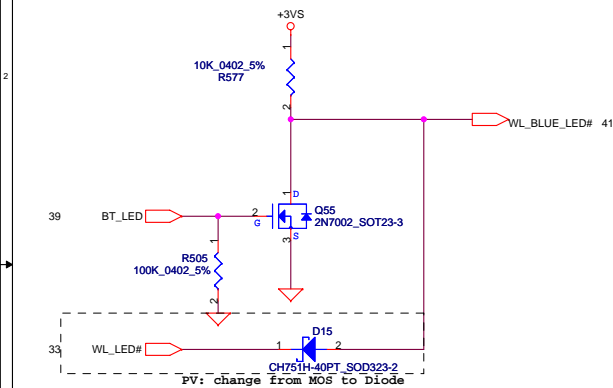
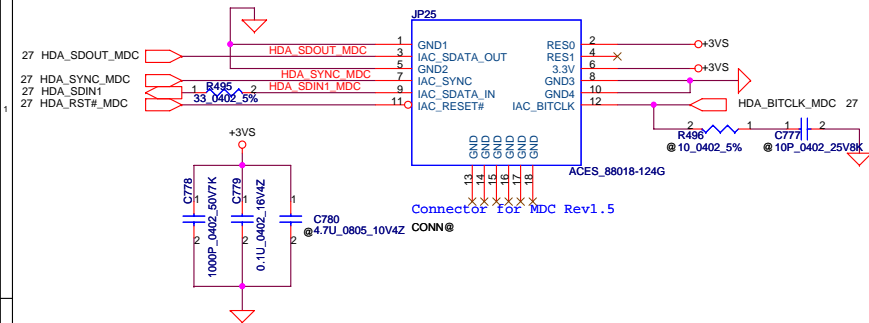
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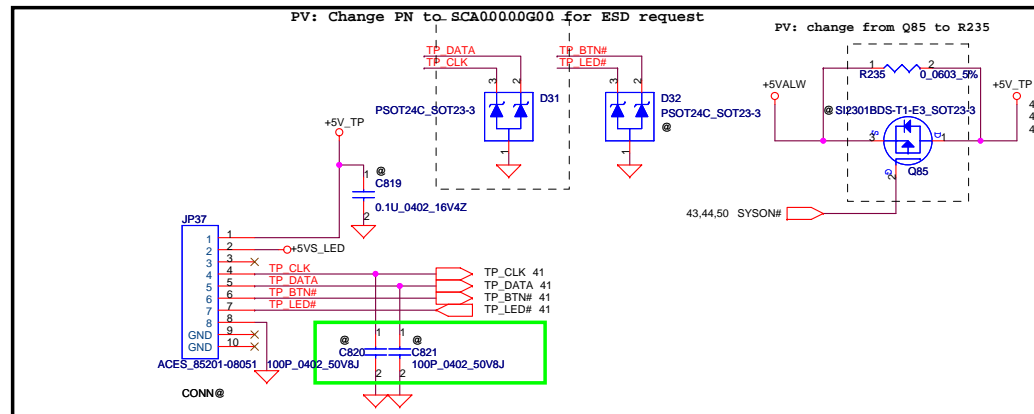
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MDC 1.5 Conn.

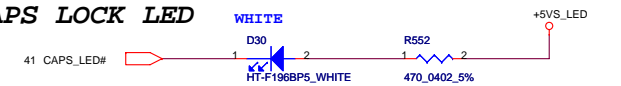
Change type 4/25



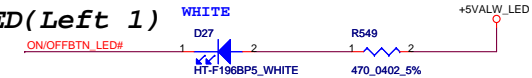
T/P Board (Include T/P_ON/OFF)



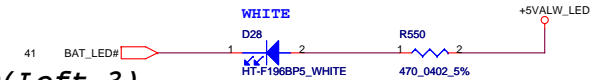
CAPS LOCK LED



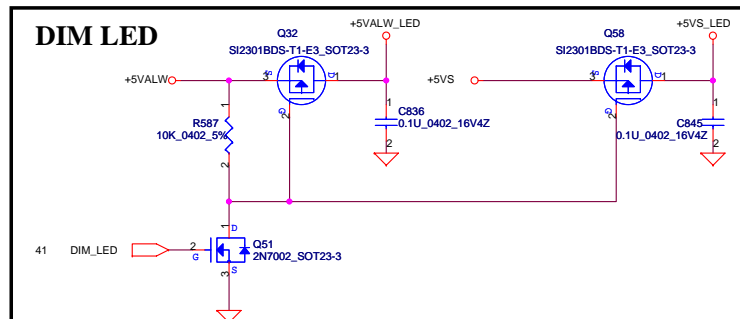
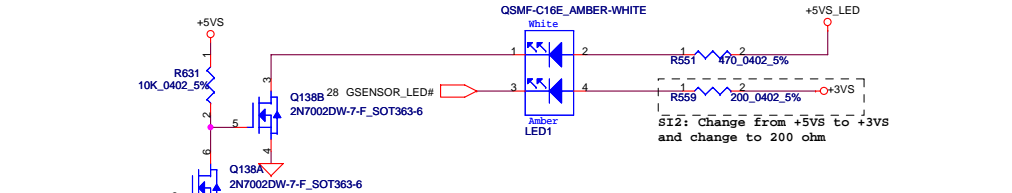
POWER LED(Left 1)



Battery Charge LED(Left 2)

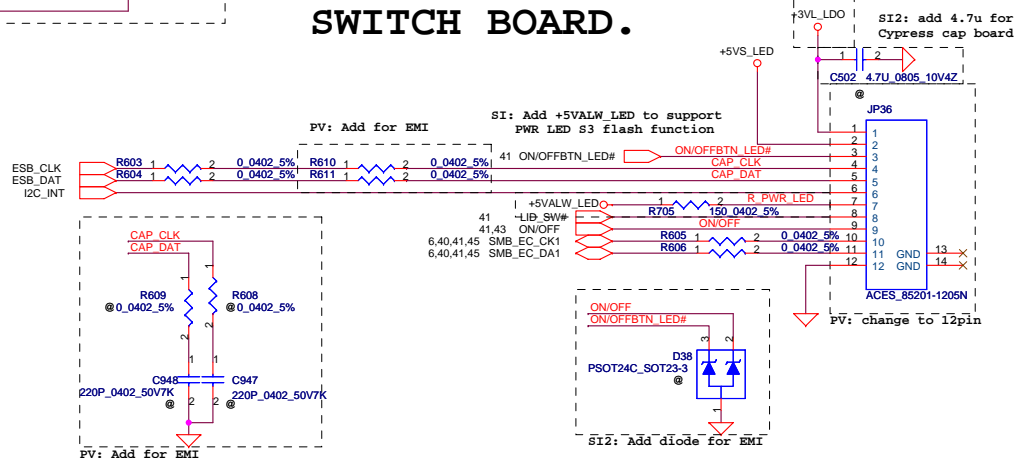


HDD LED(Left 3)



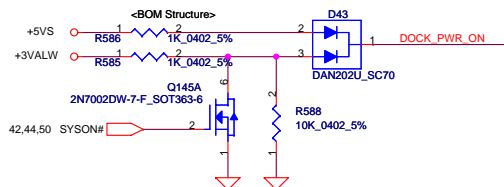
SI: Change to +3VL to support Qplay bottom boot in BATT mode

SWITCH BOARD.



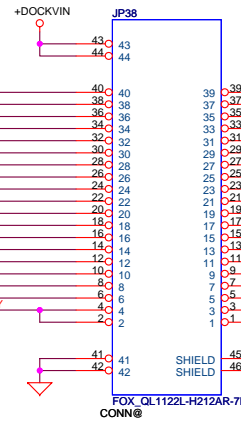
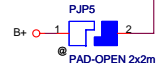
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Atlas/ Saturn Dock

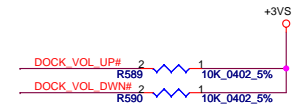


DOCK_PWR_ON Spec
0V = Notebook S4/S5, Dock off
2.5V = Notebook S3, Dock on
4V = Notebook S0, Dock on

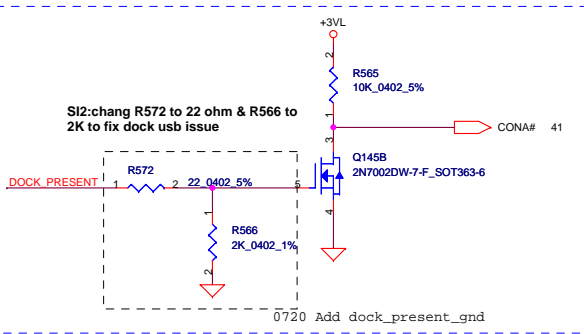
23 GREEN_L
23 RED_L
23 BLUE_L
23 D_HSYNC
23 D_DDCCLK
27 USB20_N3
23 D_VSYNC
27 USB20_P3
32 RJ45_MIDI3+
32 RJ45_MIDI3-
32 RJ45_MIDI2+
32 RJ45_MIDI2-
32 RJ45_MIDI1+
32 RJ45_MIDI1-
32 RJ45_MIDI0+
32 RJ45_MIDI0-



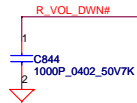
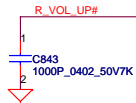
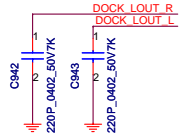
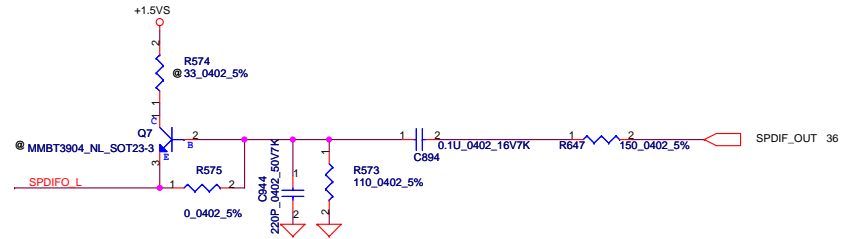
need change to reverse type connector



MUTE_LED 41
DOCK_SLP_BTN# 41,42
JACK_DET# 36,37
DOCK_VOL_UP# 41
DOCK_VOL_DWN# 41

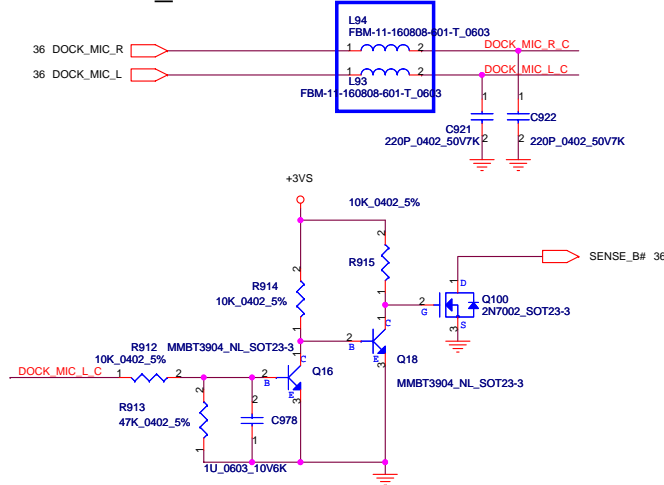


0720 Add dock_present_gnd



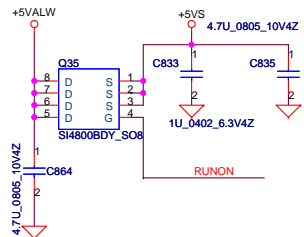
MIC_Dock

Need 600 Ohm 500 mA

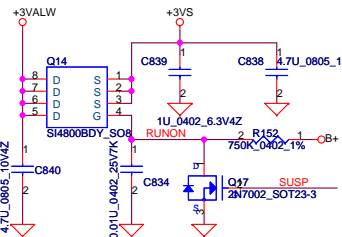


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				DOCK CONN	

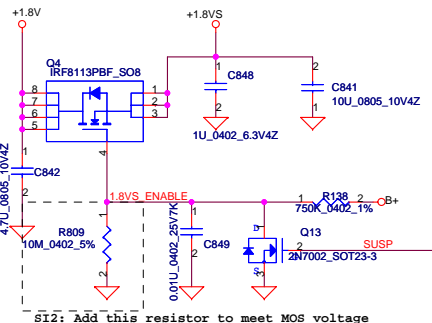
+5VALW TO +5VS



+3VALW TO +3VS

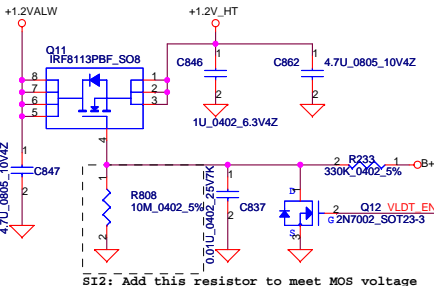


+1.8V TO +1.8VS

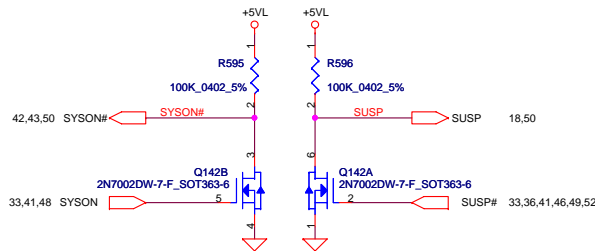
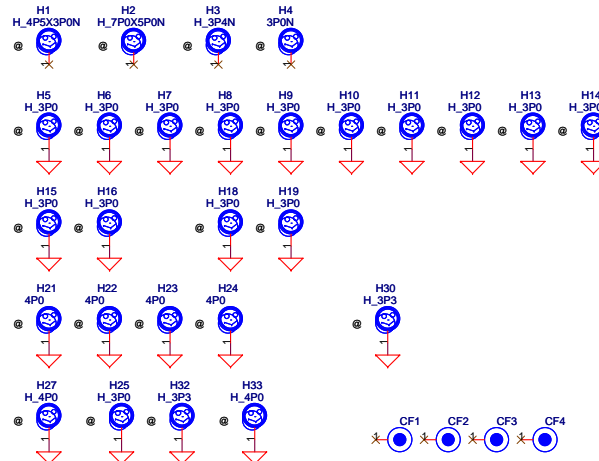


SI2: Add this resistor to meet MOS voltage

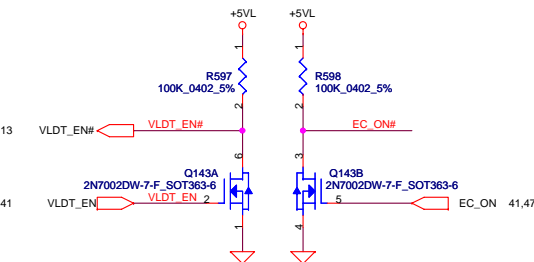
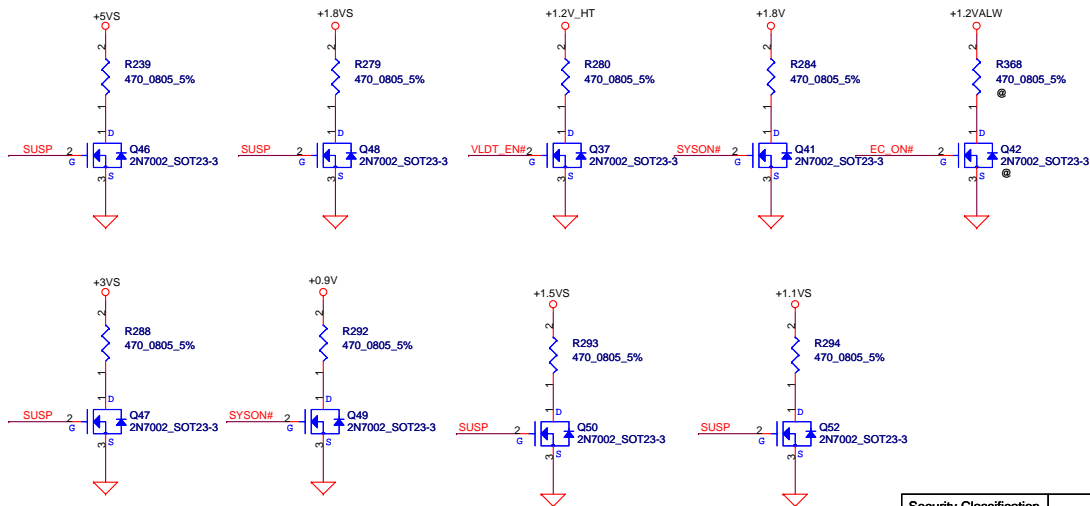
+1.2VALW TO +1.2V_HT



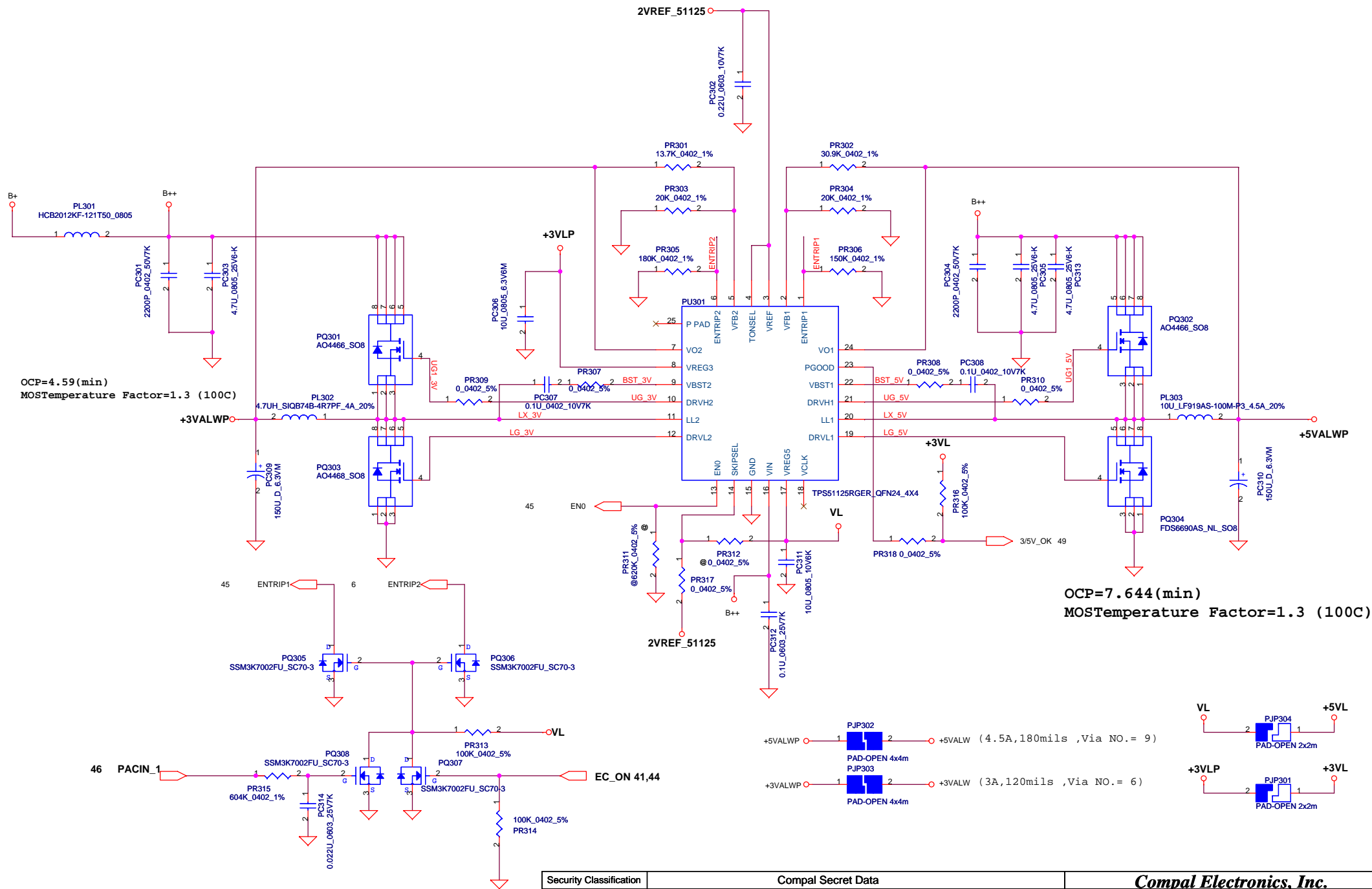
SI2: Add this resistor to meet MOS voltage



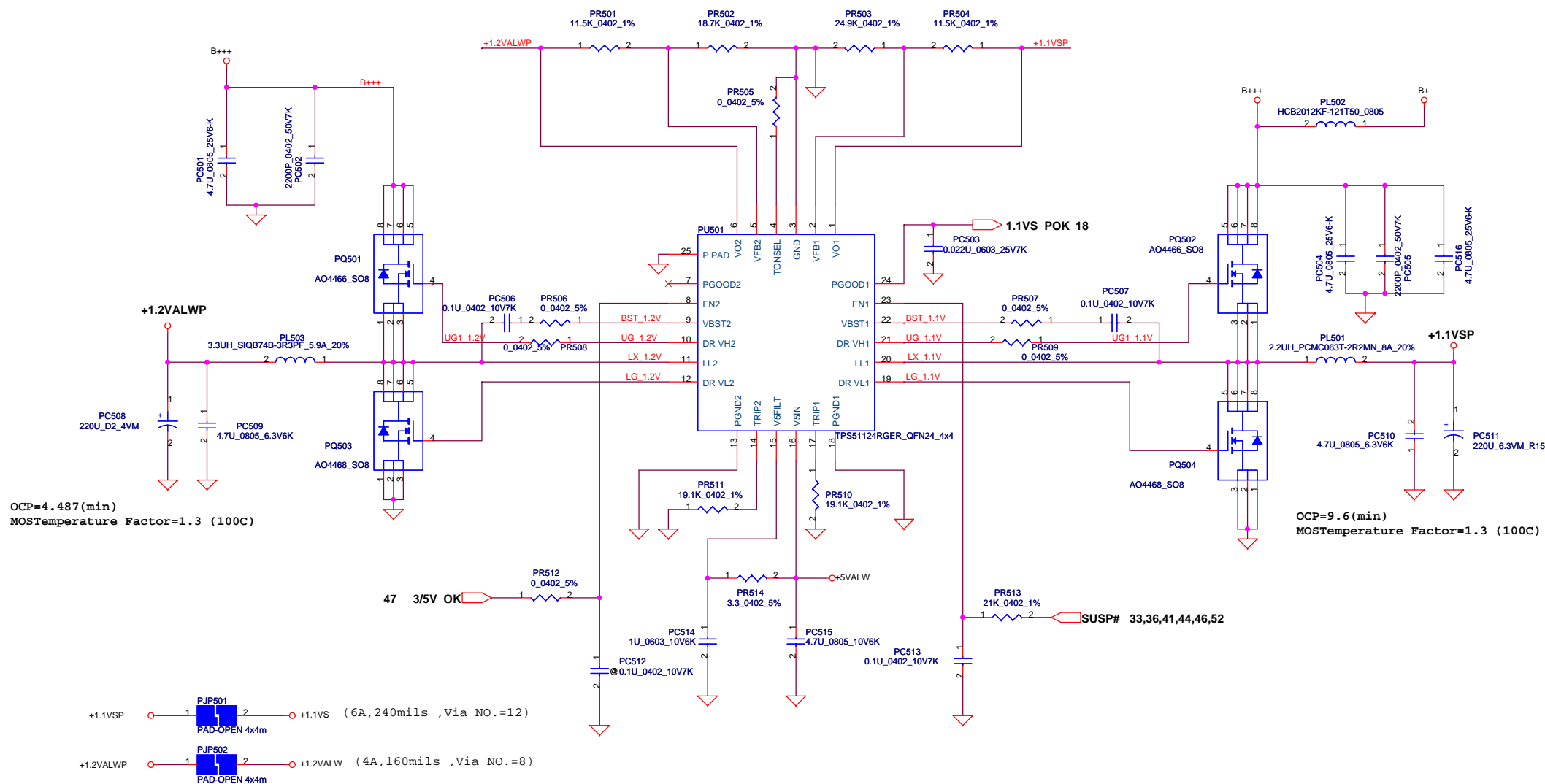
Discharge circuit



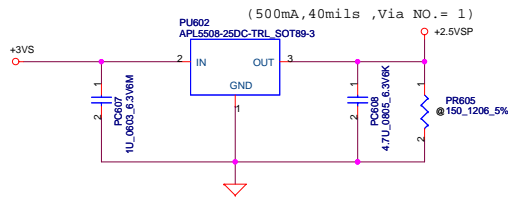
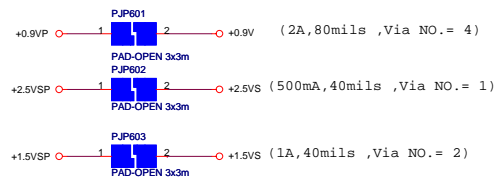
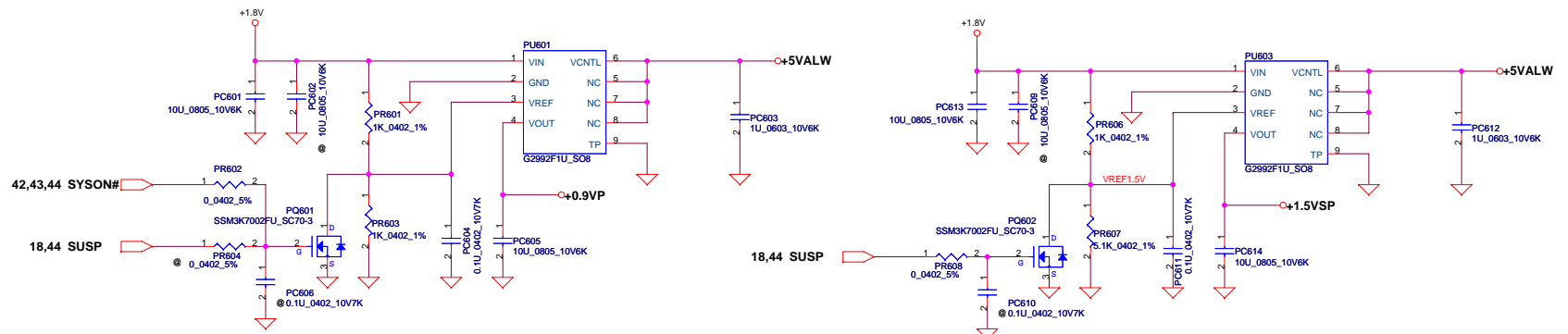
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Issued Date	2007/08/02	Deciphered Date	2008/08/02	DC/DC Circuits	
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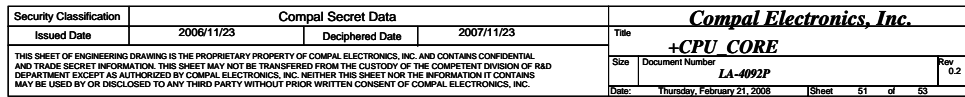
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Version Change List (P. I. R. List)for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	48	1.8VP	10/23	Compal	for power request	PU401 change the IC from "S IC RT8204PQW WQFN 16P" to "S IC TPS51117RGYR QFN 14P".	
2	46	Charger	10/30	Compal	for power request	PQ104 swap the PQ104 1,3 Pin	
3	47	3V/5V	10/30	Compal	for power request	Change PR301 to 13.7K modify output voltage	
4	47	3V/5V	10/30	Compal	for power request	Change PR305 to 180K modify OCP	
5	47	3V/5V	10/30	Compal	for power request	Change PR306 to 150K modify OCP	
6	47	3V/5V	10/30	Compal	for power request	Change PR311 to 620K	
7	47	3V/5V	10/30	Compal	for power request	Change PR315 to 604K modify sequence	
8	49	+1.1VSP	10/30	Compal	for power request	Change PR510 to 19.1K modify OCP	
9	49	+1.2VALWP	10/30	Compal	for power request	Change PR511 to 19.1K modify OCP	
10	46	Charger	10/30	Compal	for power request	Del PR119	
11	51	CPU_CORE	10/30	Compal	for power request	Change PC202 to B2 type for ME limit	
12	51	CPU_CORE	10/30	Compal	for power request	Change PR223 to 17.8K and PR224 to 100K modify OCP	
13	51	CPU_CORE	10/30	Compal	for power request	Change PR221,PR231 to 16.5K and PR217,PR233 to 4.02K for CPU_CORE compensation	
14	45	DC connector	10/30	Compal	for power request	Add PR3,PD4,PC12 for ADP_ID function	
15	47	3V/5V	10/30	Compal	for power request	Add PR317,PR318	
16	46	Charger	10/30	Compal	for power request	Change net from +3VLP to +3VL	
17	49	+1.1VSP	10/30	Compal	for power request	Change PR513 to 21K for HW power scquence.	
18	46	Charger	11/09	Compal	for power request	Pop PR119 Unpop PR9	
19	50	0.9VSP	11/09	Compal	for power request	Change PC601,PC605,PC611,PC603,PC613,PC614,PC612, PC201 for common part	
20	46	Charger	11/09	Compal	for power request	Change PR112 to 0.015 Ohm	
21	49	+1.2VALWP	11/09	Compal	for power request	Change PC508 to D2 size for ME limit	
22	51	CPU_CORE	12/05	Compal	for EMI request	Add PR220,PR229 for EMI	
23	49	CPU_CORE	12/05	Compal	for EMI request	Add PC218,PC226 for EMI	

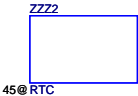
Version Change List (P. I. R. List) for Power Circuit

Item	Page#	Title	Date	Request Owner	Issue Description	Solution Description	Rev.
1	46	Charger	12/05	Compal	for power request	Change PR120 to 133K to change charger current	
2	47	3V/5V	12/05	Compal	for power request	Change PR302 to 30.9K for common part	
3	47	3V/5V	12/05	Compal	for power request	Change PR304 to 20K for common part	
4	48	+1.8VP	12/05	Compal	for power request	Change PR408 to 18.2K modify OCP	
5	52	VGA_CORE	12/05	Compal	for power request	Change PR306 to 150K modify OCP	
6	52	VGA_CORE	12/05	Compal	for power request	Change PR714 to 0 Ohm	
7	52	VGA_CORE	12/05	Compal	for power request	Add PR713 100 Ohm	
8	45	DC Connector /CPU_OTP	12/25	Compal	for power request	Del PR9	
9	46	Charger	12/25	Compal	for power request	Reconnect from BQ24740VREF to +3VL	
10	47	3V/5V	12/25	Compal	for power request	Add PU302	
11	52	VGA_CORE	12/25	Compal	for power request	Del PC714 Change PC715 to 0.022u & PR713 to 10 Ohm	
12	51	CPU_CORE	12/27	Compal	for power request	ADD PC204 & PC211 68uF	
13	48	+1.8VP	1/2	Compal	for EMI request	Add PR410 4.7ohm and PC410 680P	
14	48	+1.8VP	1/2	Compal	for EMI request	Add PC405 680P and 408 3.3nF	
15	51	CPU_CORE	1/2	Compal	for EMI request	ADD PC241 820p & PC242 3300p	
16	52	VGA_CORE	1/2	Compal	for EMI request	Add PR710 and PC709	
17	51	CPU_CORE	1/2	Compal	for EMI request	ADD PC243 to 3.3n PC244 to 820p	
18	51	CPU_CORE	1/3	Compal	for power request	ADD PR234 & PQ115	

HW4 Product Improvement Record (P.I.R.)

- 1. Change R538 Pull high from +3VL to +3VALW
- 2. New add R563,R571 Pull high +3VS
- 3. Unmount BKOFF# Pull high R483
- 4. Unmount CPU_LDT_REQ# Pull high R318
- 5. Change LED1 P/N to SC500004C00
- 6. Change JP36 Pin2 from +5VS_LED to +5VALW_LED
- 7. Change C1012 & C1013 from 4700P to 1000P
- 8. Change R186 size from 0603 to 0402
- 9. Delete TV function and relation component
- 10. Add R554 for CIR pull high
- 11.Add C327 on BATT_OVT
- 12.Change L57 & L59 to 0603 BLM18PG121SN1D
- 13. exchange TV & WLAN mini card location
- 14.add LAN cable detect circuit
- 15.update ODD CONN footporint and symbol
- 16.delete Lid switch baord Conn
- 17.Change Cap sensor board power to +3VL to support Qplay boot

RTC



PCB



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